

# DATA SHEET

For a complete data sheet, please also download:

- The IC06 74HC/HCT/HCU/HCMOS Logic Family Specifications
- The IC06 74HC/HCT/HCU/HCMOS Logic Package Information
- The IC06 74HC/HCT/HCU/HCMOS Logic Package Outlines

## **74HC/HCT563**

**Octal D-type transparent latch;  
3-state; inverting**

Product specification  
File under Integrated Circuits, IC06

December 1990

# Octal D-type transparent latch; 3-state; inverting

## 74HC/HCT563

### FEATURES

- 3-state inverting outputs for bus oriented applications
- Inputs and outputs on opposite sides of package allowing easy interface with microprocessor
- Common 3-state output enable input
- Output capability: bus driver
- I<sub>CC</sub> category: MSI

### GENERAL DESCRIPTION

The 74HC/HCT563 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky

TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7A.

The 74HC/HCT563 are octal D-type transparent latches featuring separate D-type inputs for each latch and inverting 3-state outputs for bus oriented applications.

A latch enable (LE) input and an output enable ( $\overline{OE}$ ) input are common to all latches.

The "563" is functionally identical to the "573", but has inverted outputs.

The "563" consists of eight D-type transparent latches with 3-state inverting outputs. The LE and  $\overline{OE}$  are

common to all latches.

When LE is HIGH, data at the D<sub>n</sub> inputs enter the latches. In this condition the latches are transparent, i.e. a latch output will change state each time its corresponding D-input changes.

When LE is LOW the latches store the information that was present at the D-inputs a set-up time preceding the HIGH-to-LOW transition of LE.

When  $\overline{OE}$  is LOW, the contents of the 8 latches are available at the outputs. When  $\overline{OE}$  is HIGH, the outputs go to the high impedance OFF-state.

Operation of the  $\overline{OE}$  input does not affect the state of the latches.

### QUICK REFERENCE DATA

GND = 0 V; T<sub>amb</sub> = 25 °C; t<sub>r</sub> = t<sub>f</sub> = 6 ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay D <sub>n</sub> , LE to $\overline{Q}_n$	C <sub>L</sub> = 15 pF; V <sub>CC</sub> = 5 V	14	16	ns
C <sub>I</sub>	input capacitance		3.5	3.5	pF
C <sub>PD</sub>	power dissipation capacitance per latch	notes 1 and 2	19	19	pF

### Notes

1. C<sub>PD</sub> is used to determine the dynamic power dissipation (P<sub>D</sub> in μW):

$$P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum (C_L \times V_{CC}^2 \times f_o) \text{ where:}$$

f<sub>i</sub> = input frequency in MHz

f<sub>o</sub> = output frequency in MHz

$\sum (C_L \times V_{CC}^2 \times f_o)$  = sum of outputs

C<sub>L</sub> = output load capacitance in pF

V<sub>CC</sub> = supply voltage in V

2. For HC the condition is V<sub>I</sub> = GND to V<sub>CC</sub>  
for HCT the condition is V<sub>I</sub> = GND to V<sub>CC</sub> - 1.5 V

### ORDERING INFORMATION

See "74HC/HCT/HCU/HCMOS Logic Package Information".

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PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
2, 3, 4, 5, 6, 7, 8, 9	D <sub>0</sub> to D <sub>7</sub>	data inputs
11	LE	latch enable input (active HIGH)
1	$\overline{OE}$	3-state output enable input (active LOW)
10	GND	ground (0 V)
19, 18, 17, 16, 15, 14, 13, 12	$\overline{Q}_0$ to $\overline{Q}_7$	3-state latch outputs
20	V <sub>CC</sub>	positive supply voltage

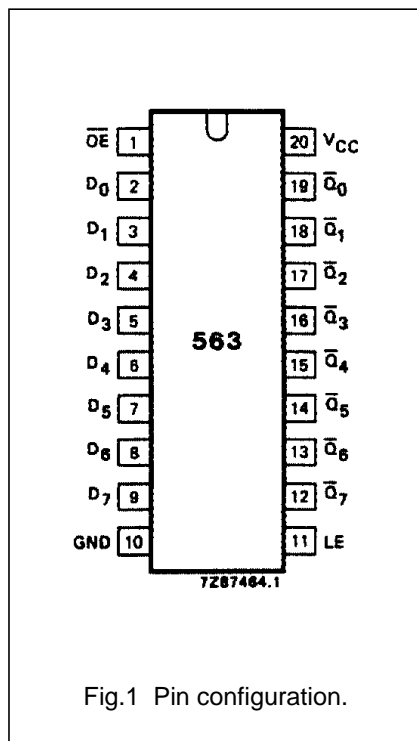


Fig.1 Pin configuration.

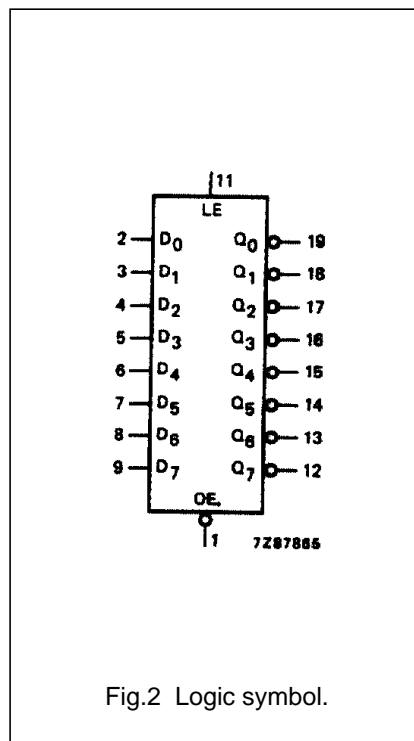


Fig.2 Logic symbol.

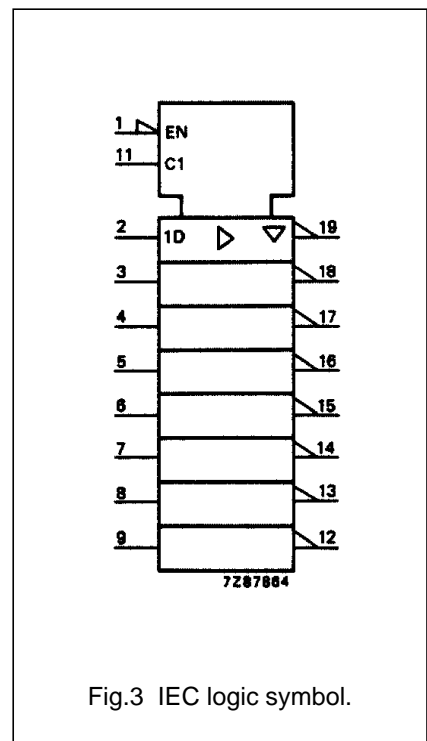


Fig.3 IEC logic symbol.

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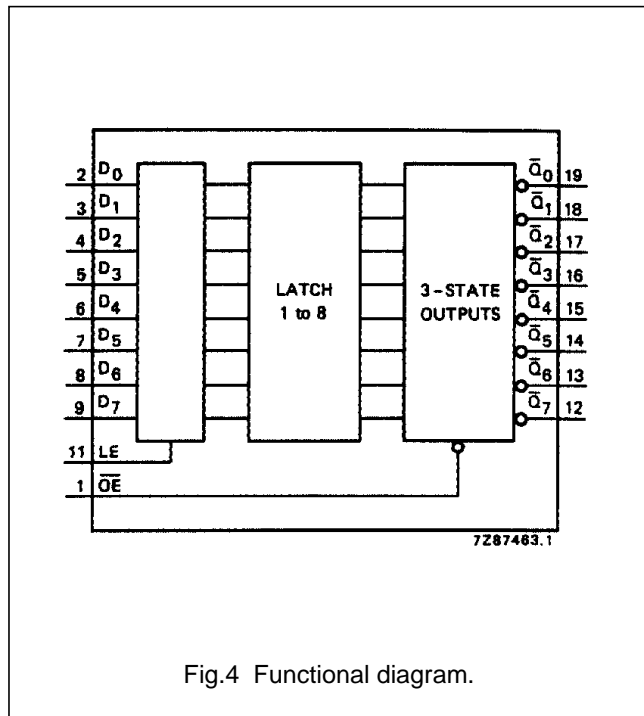


Fig.4 Functional diagram.

### FUNCTION TABLE

OPERATING MODES	INPUTS			INTERNAL LATCHES	OUTPUTS
	$\overline{OE}$	LE	$D_n$		$\overline{Q}_0$ to $\overline{Q}_7$
enable and read register	L	H	L	L	H
	L	H	H	H	L
latch and read register	L	L	l	L	H
	L	L	h	H	L
latch register and disable outputs	H	L	l	L	Z
	H	L	h	H	Z

### Notes

- H = HIGH voltage level  
 h = HIGH voltage level one set-up time prior to the HIGH-to-LOW LE transition  
 L = LOW voltage level  
 l = LOW voltage level one set-up time prior to the HIGH-to-LOW LE transition  
 Z = high impedance OFF-state

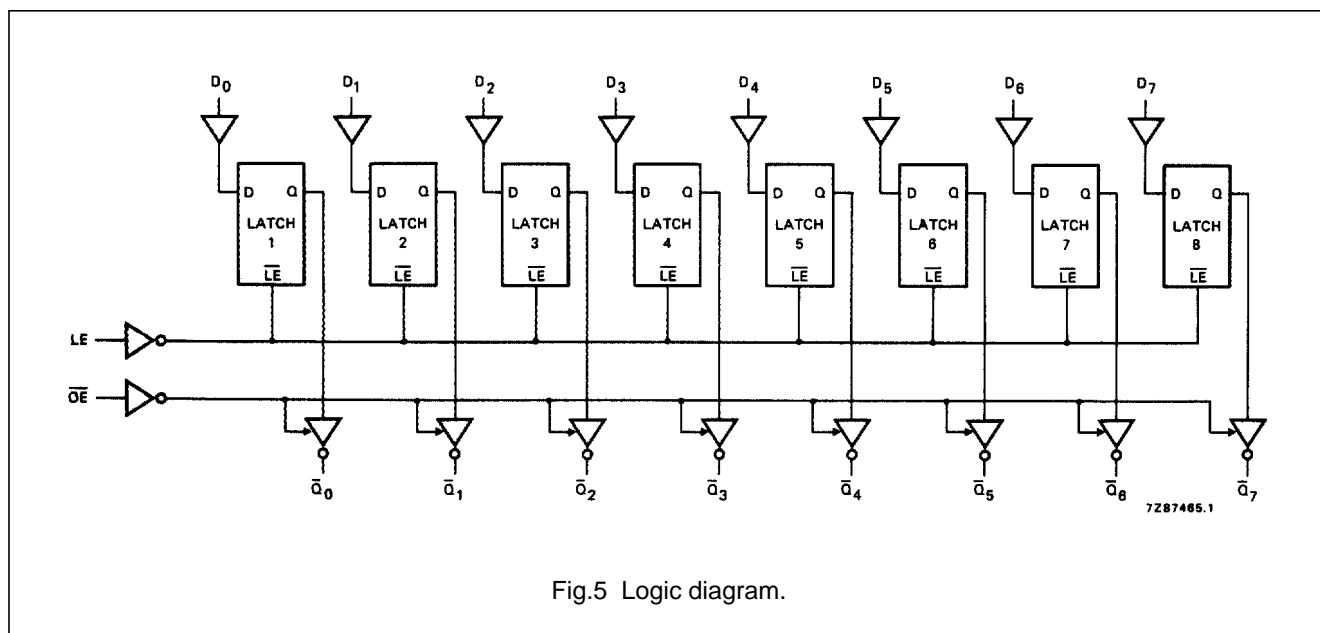


Fig.5 Logic diagram.

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## DC CHARACTERISTICS FOR 74HC

For the DC characteristics see *"74HC/HCT/HCU/HCMOS Logic Family Specifications"*.

Output capability: bus driver

I<sub>CC</sub> category: MSI

## AC CHARACTERISTICS FOR 74HC

GND = 0 V; t<sub>r</sub> = t<sub>f</sub> = 6 ns; C<sub>L</sub> = 50 pF

SYMBOL	PARAMETER	T <sub>amb</sub> (°C)						UNIT	TEST CONDITIONS		
		74HC							V <sub>CC</sub> (V)	WAVEFORMS	
		+25			-40 to +85		-40 to +125				
		min.	typ.	max.	min.	max.	min.				max.
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay D <sub>n</sub> to $\overline{Q}_n$		47 17 14	145 29 25		180 36 31		220 44 38	ns	2.0 4.5 6.0	Fig.6
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay LE to $\overline{Q}_n$		47 17 14	145 29 25		180 36 31		220 44 38	ns	2.0 4.5 6.0	Fig.7
t <sub>PZH</sub> / t <sub>PZL</sub>	3-state output enable time $\overline{OE}$ to $\overline{Q}_n$		47 17 14	150 30 26		190 38 33		225 45 38	ns	2.0 4.5 6.0	Fig.8
t <sub>PHZ</sub> / t <sub>PLZ</sub>	3-state output disable time $\overline{OE}$ to $\overline{Q}_n$		50 18 14	150 30 26		190 38 33		225 45 38	ns	2.0 4.5 6.0	Fig.8
t <sub>THL</sub> / t <sub>TLH</sub>	output transition time		14 5 4	60 12 10		75 15 13		90 18 15	ns	2.0 4.5 6.0	Fig.6
t <sub>W</sub>	enable pulse width HIGH	80 16 14	14 5 4		100 20 17		120 24 20		ns	2.0 4.5 6.0	Fig.7
t <sub>SU</sub>	set-up time D <sub>n</sub> to LE	50 10 9	11 4 3		65 13 11		75 15 13		ns	2.0 4.5 6.0	Fig.9
t <sub>H</sub>	hold time D <sub>n</sub> to LE	4 4 4	-6 -2 -2		4 4 4		4 4 4		ns	2.0 4.5 6.0	Fig.9

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## DC CHARACTERISTICS FOR 74HCT

For the DC characteristics see *"74HC/HCT/HCU/HCMOS Logic Family Specifications"*.

Output capability: bus driver

I<sub>CC</sub> category: MSI

### Note to HCT types

The value of additional quiescent supply current ( $\Delta I_{CC}$ ) for a unit load of 1 is given in the family specifications. To determine  $\Delta I_{CC}$  per input, multiply this value by the unit load coefficient shown in the table below.

INPUT	UNIT LOAD COEFFICIENT
D <sub>n</sub>	0.35
LE	0.65
$\overline{OE}$	1.25

## AC CHARACTERISTICS FOR 74HCT

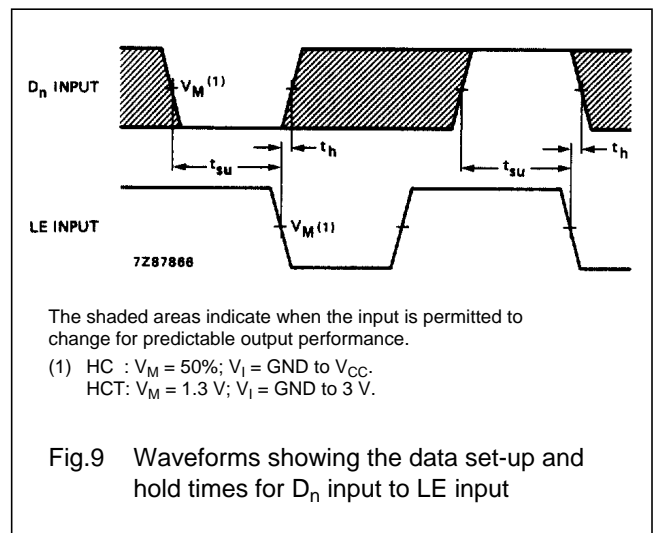
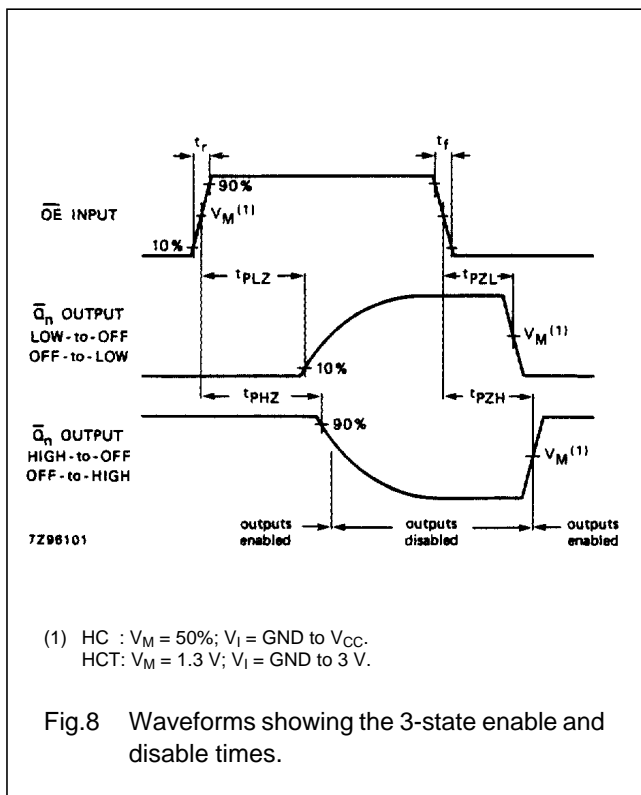
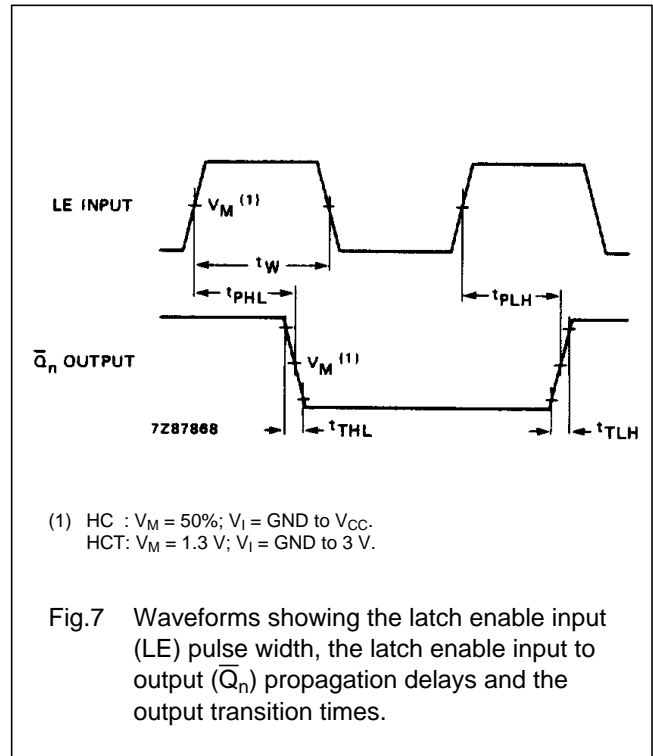
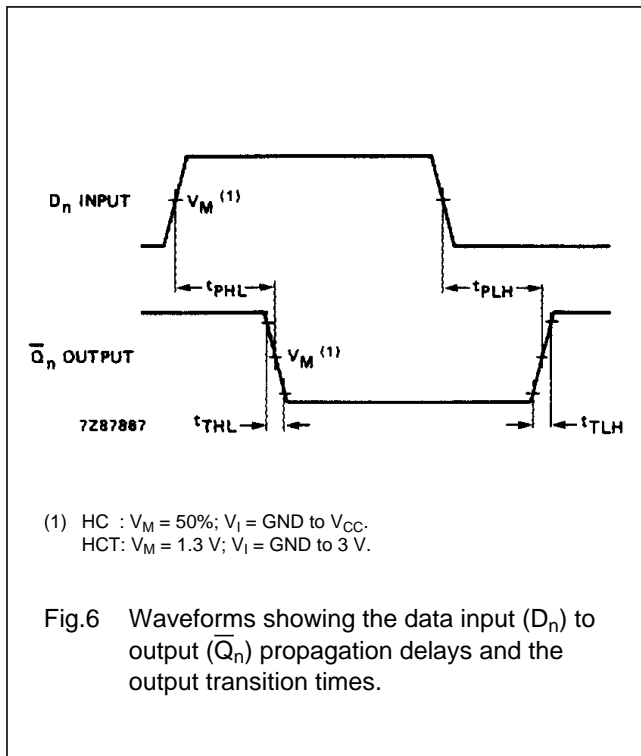
GND = 0 V; t<sub>r</sub> = t<sub>f</sub> = 6 ns; C<sub>L</sub> = 50 pF

SYMBOL	PARAMETER	T <sub>amb</sub> (°C)						UNIT	TEST CONDITIONS		
		74HCT							V <sub>CC</sub> (V)	WAVEFORMS	
		+25			-40 to +85		-40 to +125				
		min.	typ.	max.	min.	max.	min.				max.
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay D <sub>n</sub> to $\overline{Q}_n$		18	30		38		45	ns	4.5	Fig.6
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay LE to $\overline{Q}_n$		19	35		44		53	ns	4.5	Fig.7
t <sub>PZH</sub> / t <sub>PZL</sub>	3-state output enable time $\overline{OE}$ to $\overline{Q}_n$		20	35		44		53	ns	4.5	Fig.8
t <sub>PHZ</sub> / t <sub>PLZ</sub>	3-state output disable time $\overline{OE}$ to $\overline{Q}_n$		22	35		44		53	ns	4.5	Fig.8
t <sub>THL</sub> / t <sub>TLH</sub>	output transition time		5	12		15		18	ns	4.5	Fig.6
t <sub>W</sub>	enable pulse width HIGH	16	5		20		24		ns	4.5	Fig.7
t <sub>SU</sub>	set-up time D <sub>n</sub> to LE	10	3		13		15		ns	4.5	Fig.9
t <sub>H</sub>	hold time D <sub>n</sub> to LE	5	-1		5		5		ns	4.5	Fig.9

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AC WAVEFORMS



PACKAGE OUTLINES

See "74HC/HCT/HCU/HCMOS Logic Package Outlines".