

# DATA SHEET

For a complete data sheet, please also download:

- The IC06 74HC/HCT/HCU/HCMOS Logic Family Specifications
- The IC06 74HC/HCT/HCU/HCMOS Logic Package Information
- The IC06 74HC/HCT/HCU/HCMOS Logic Package Outlines

## **74HC/HCT242**

**Quad bus transceiver; 3-state;  
inverting**

Product specification  
File under Integrated Circuits, IC06

December 1990

## Quad bus transceiver; 3-state; inverting

## 74HC/HCT242

## FEATURES

- Inverting 3-state outputs
- 2-way asynchronous data bus communication
- Output capability: bus driver
- I<sub>CC</sub> category: MSI

## GENERAL DESCRIPTION

The 74HC/HCT242 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL

(LSTTL). They are specified in compliance with JEDEC standard no. 7A.

The 74HC/HCT242 are quad bus transceivers featuring inverting 3-state bus compatible outputs in both send and receive directions.

They are designed for 4-line asynchronous 2-way data communications between data buses.

The output enable inputs ( $\overline{OE}_A$  and  $OE_B$ ) can be used to isolate the buses.

The "242" is similar to the "243" but has inverting outputs.

## QUICK REFERENCE DATA

GND = 0 V; T<sub>amb</sub> = 25 °C; t<sub>r</sub> = t<sub>f</sub> = 6 ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay A <sub>n</sub> to B <sub>n</sub> ; B <sub>n</sub> to A <sub>n</sub>	C <sub>L</sub> = 15 pF; V <sub>CC</sub> = 5 V	7	10	ns
C <sub>I</sub>	input capacitance		3.5	3.5	pF
C <sub>I/O</sub>	input/output capacitance		10	10	pF
C <sub>PD</sub>	power dissipation capacitance per transceiver	notes 1 and 2	29	32	pF

## Notes

1. C<sub>PD</sub> is used to determine the dynamic power dissipation (P<sub>D</sub> in μW):

$$P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum (C_L \times V_{CC}^2 \times f_o) \text{ where:}$$

f<sub>i</sub> = input frequency in MHz

f<sub>o</sub> = output frequency in MHz

∑ (C<sub>L</sub> × V<sub>CC</sub><sup>2</sup> × f<sub>o</sub>) = sum of outputs

C<sub>L</sub> = output load capacitance in pF

V<sub>CC</sub> = supply voltage in V

2. For HC the condition is V<sub>I</sub> = GND to V<sub>CC</sub>  
For HCT the condition is V<sub>I</sub> = GND to V<sub>CC</sub> – 1.5 V

## ORDERING INFORMATION

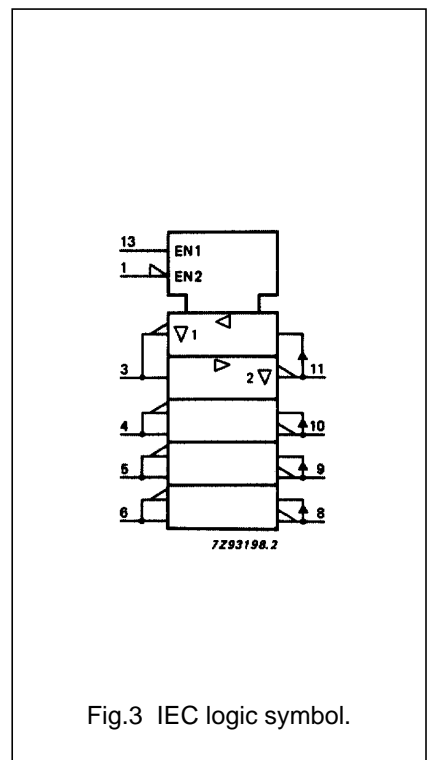
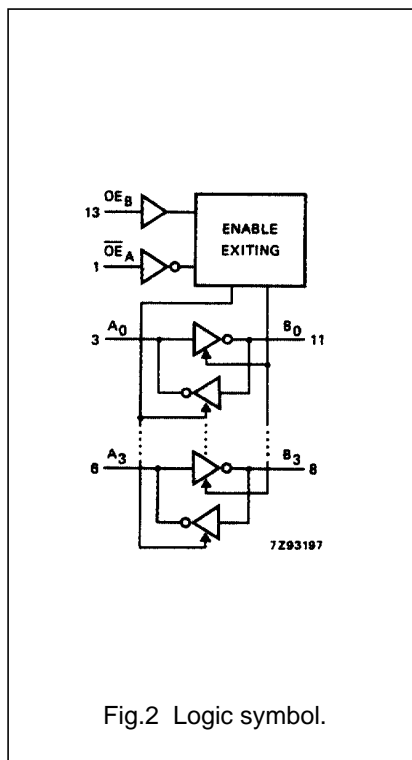
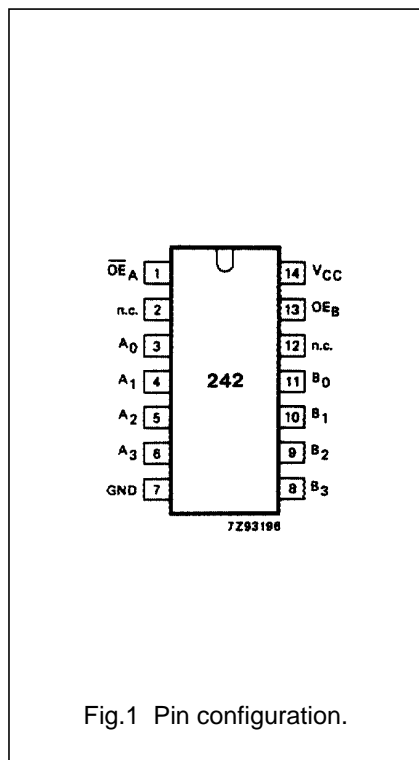
See "74HC/HCT/HCU/HCMOS Logic Package Information".

Quad bus transceiver; 3-state; inverting

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PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
1	$\overline{OE}_A$	output enable input (active LOW)
2, 12	n.c.	not connected
3, 4, 5, 6	$A_0$ to $A_3$	data inputs/outputs
7	GND	ground (0 V)
11, 10, 9, 8	$B_0$ to $B_3$	data inputs/outputs
13	$OE_B$	output enable input
14	$V_{CC}$	positive supply voltage



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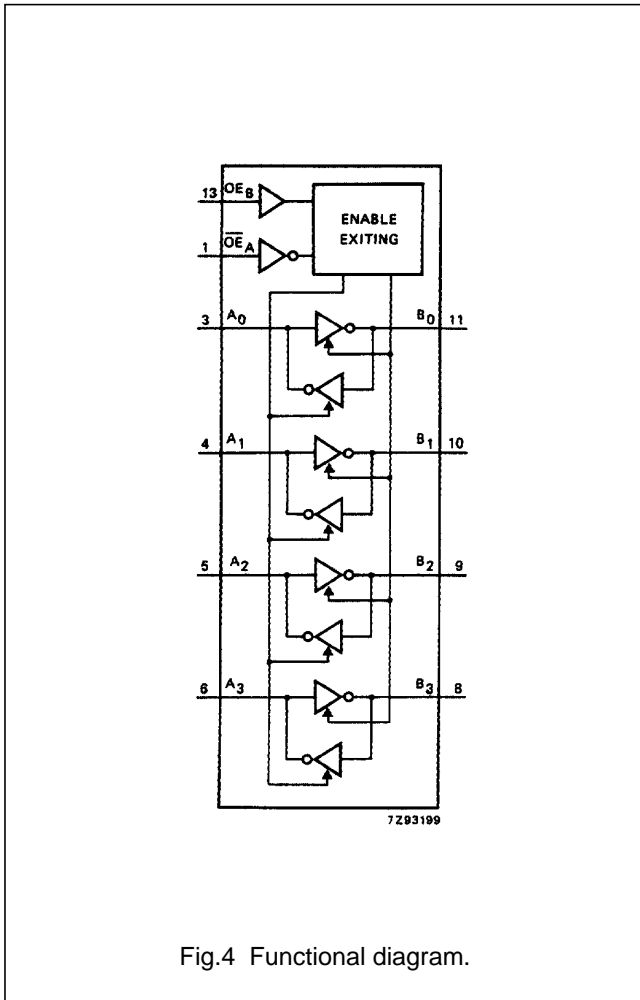


Fig.4 Functional diagram.

FUNCTION TABLE

INPUTS		INPUTS/OUTPUTS	
$\overline{OE}_A$	$OE_B$	$A_n$	$B_n$
L	L	inputs	$B = \overline{A}$
H	L	Z	Z
L	H	Z	Z
H	H	$A = \overline{B}$	inputs

Note

- H = HIGH voltage level  
L = LOW voltage level  
Z = high impedance OFF-state

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**DC CHARACTERISTICS FOR 74HC**

For the DC characteristics see *"74HC/HCT/HCU/HCMOS Logic Family Specifications"*.

Output capability: bus driver

I<sub>CC</sub> category: MSI

**AC CHARACTERISTICS FOR 74HC**

GND = 0 V; t<sub>r</sub> = t<sub>f</sub> = 6 ns; C<sub>L</sub> = 50 pF

SYMBOL	PARAMETER	T <sub>amb</sub> (°C)						UNIT	TEST CONDITIONS		
		74HC							V <sub>CC</sub> (V)	WAVEFORMS	
		+25			-40 to +85		-40 to +125				
		min.	typ.	max.	min.	max.	min.				max.
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay A <sub>n</sub> to B <sub>n</sub> ; B <sub>n</sub> to A <sub>n</sub>		25 9 7	90 18 15		115 23 20		135 27 23	ns	2.0 4.5 6.0	Fig.5
t <sub>PZH</sub> / t <sub>PZL</sub>	3-state output enable time $\overline{OE}_A$ to A <sub>n</sub> or B <sub>n</sub> ; OE <sub>B</sub> to A <sub>n</sub> or B <sub>n</sub>		41 15 12	150 30 26		190 38 33		225 45 38	ns	2.0 4.5 6.0	Figs 6 and 7
t <sub>PHZ</sub> / t <sub>PLZ</sub>	3-state output disable time $\overline{OE}_A$ to A <sub>n</sub> or B <sub>n</sub> ; OE <sub>B</sub> to A <sub>n</sub> or B <sub>n</sub>		52 19 15	150 30 26		190 38 33		225 45 38	ns	2.0 4.5 6.0	Figs 6 and 7
t <sub>THL</sub> / t <sub>TLH</sub>	output transition time		14 5 4	60 12 10		75 15 13		90 18 15	ns	2.0 4.5 6.0	Fig.5

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## 74HC/HCT242

**DC CHARACTERISTICS FOR 74HCT**

For the DC characteristics see *"74HC/HCT/HCU/HCMOS Logic Family Specifications"*.

Output capability: bus driver

I<sub>CC</sub> category: MSI

**Note to HCT types**

The value of additional quiescent supply current ( $\Delta I_{CC}$ ) for a unit load of 1 is given in the family specifications.

To determine  $\Delta I_{CC}$  per input, multiply this value by the unit load coefficient shown in the table below.

INPUT	UNIT LOAD COEFFICIENT
A <sub>n</sub>	1.10
B <sub>n</sub>	1.10
$\overline{OE}_A$	1.00
OE <sub>B</sub>	1.00

**AC CHARACTERISTICS FOR 74HCT**

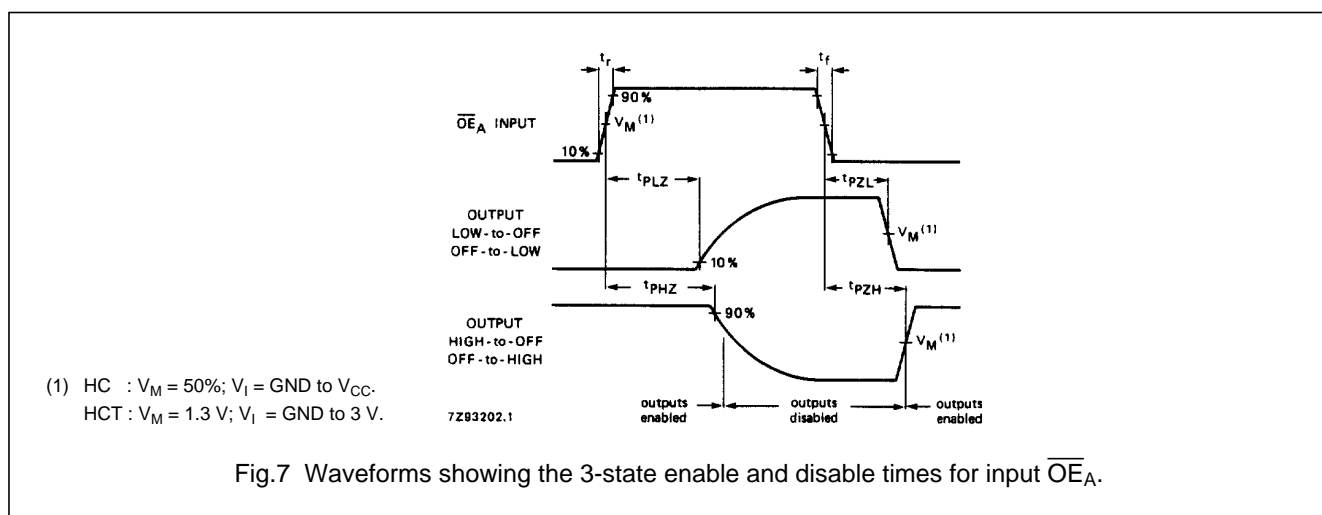
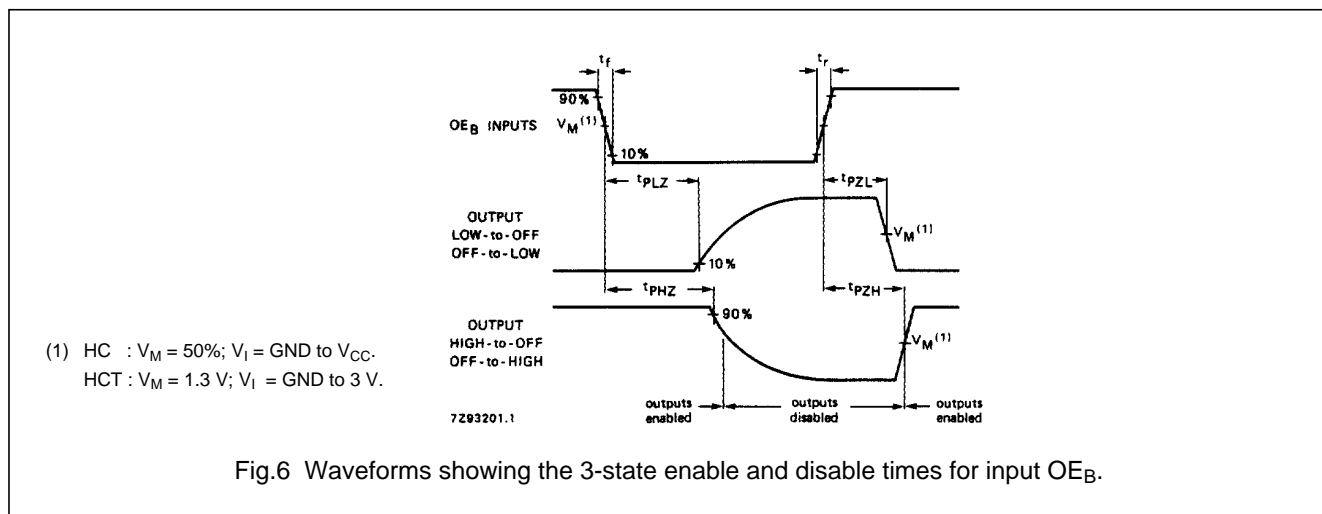
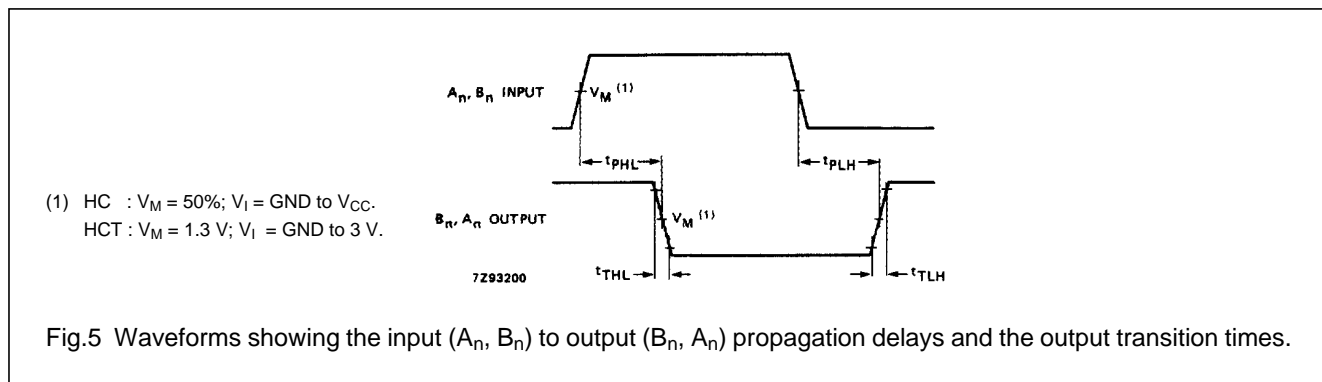
GND = 0 V; t<sub>r</sub> = t<sub>f</sub> = 6 ns; C<sub>L</sub> = 50 pF

SYMBOL	PARAMETER	T <sub>amb</sub> (°C)						UNIT	TEST CONDITIONS		
		74HCT							V <sub>CC</sub> (V)	WAVEFORMS	
		+25			-40 to +85		-40 to +125				
		min.	typ.	max.	min.	max.	min.				max.
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay A <sub>n</sub> to B <sub>n</sub> ; B <sub>n</sub> to A <sub>n</sub>		12	20		25		30	ns	4.5	Fig.5
t <sub>PZH</sub> / t <sub>PZL</sub>	3-state output enable time $\overline{OE}_A$ to A <sub>n</sub> or B <sub>n</sub> ; OE <sub>B</sub> to A <sub>n</sub> or B <sub>n</sub>		16	34		43		51	ns	4.5	Figs 6 and 7
t <sub>PHZ</sub> / t <sub>PLZ</sub>	3-state output disable time $\overline{OE}_A$ to A <sub>n</sub> or B <sub>n</sub> ; OE <sub>B</sub> to A <sub>n</sub> or B <sub>n</sub>		22	35		44		53	ns	4.5	Figs 6 and 7
t <sub>THL</sub> / t <sub>TLH</sub>	output transition time		5	12		15		18	ns	4.5	Fig.5

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AC WAVEFORMS



PACKAGE OUTLINES

See "74HC/HCT/HCU/HCMOS Logic Package Outlines".

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