

SN54HC7006, SN74HC7006 6-SECTION MULTIFUNCTION (NAND, INVERT, NOR) CIRCUITS

D2831, MARCH 1984—REVISED SEPTEMBER 1987

- Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs
- Dependable Texas Instruments Quality and Reliability

description

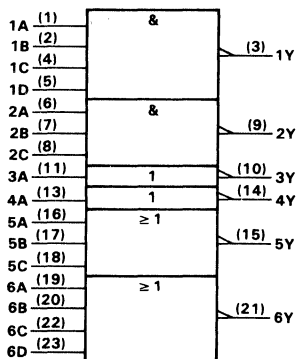
The SN54HC7006 and SN74HC7006 are each comprised of the following sections:

- One 3-input NAND gate
- One 4-input NAND gate
- One 3-input NOR gate
- One 4-input NOR gate
- Two inverters

They perform the Boolean functions shown under each function table.

The SN54HC7006 is characterized for operation over the full military temperature range of -55°C to 125°C . The SN74HC7006 is characterized for operation from -40°C to 85°C .

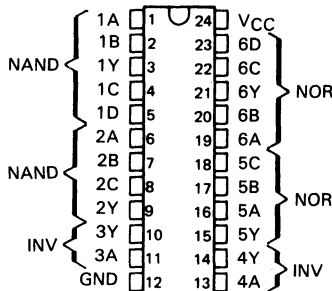
logic symbol†



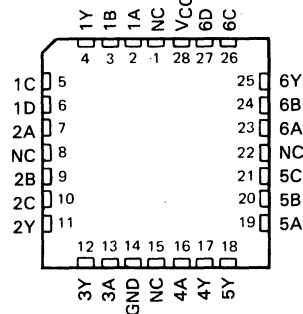
†This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

Pin numbers shown are for DW, JT, and NT packages.

SN54HC7006 . . . JT PACKAGE
SN74HC7006 . . . DW OR NT PACKAGE
(TOP VIEW)



SN54HC7006 . . . FK PACKAGE
(TOP VIEW)

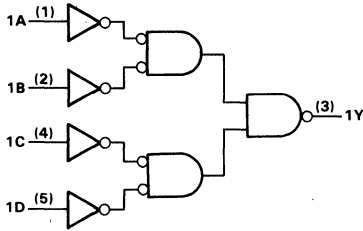


NC—No internal connection

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logic diagrams (positive logic)

4-INPUT NAND GATE

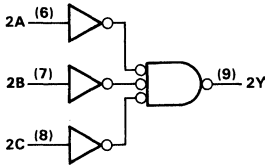


FUNCTION TABLE

INPUTS				OUTPUT Y
A	B	C	D	
H	H	H	H	L
L	X	X	X	H
X	L	X	X	H
X	X	L	X	H
X	X	X	L	H

positive logic: $Y = \overline{A \cdot B \cdot C \cdot D}$ or
 $Y = \overline{A + B + C + D}$

3-INPUT NAND GATE

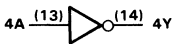
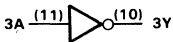


FUNCTION TABLE

INPUTS			OUTPUT Y
A	B	C	
H	H	H	L
L	X	X	H
X	L	X	H
X	X	L	H

positive logic: $Y = \overline{A \cdot B \cdot C}$ or
 $Y = \overline{A + B + C}$

INVERTERS

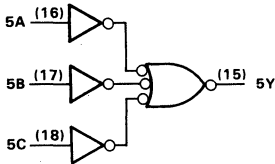


FUNCTION TABLE
(EACH INVERTER)

INPUT A	OUTPUT Y
H	L
L	H

positive logic: $Y = \overline{A}$

3-INPUT NOR GATE



FUNCTION TABLE

INPUTS			OUTPUT Y
A	B	C	
H	X	X	L
X	H	X	L
X	X	H	L
L	L	L	H

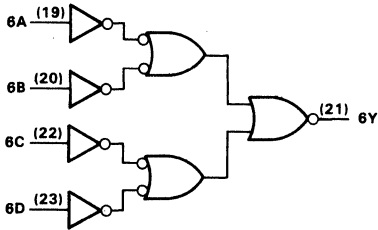
positive logic: $Y = \overline{A + B + C}$ or
 $Y = \overline{A \cdot B \cdot C}$

Pin numbers shown are for DW, JT, and NT packages.

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logic diagram (positive logic)

4-INPUT NOR GATE



FUNCTION TABLE

INPUTS				OUTPUT Y
A	B	C	D	
H	X	X	X	L
X	H	X	X	L
X	X	H	X	L
X	X	X	H	L
L	L	L	L	H

positive logic: $Y = \overline{A+B+C+D}$ or
 $Y = \overline{A} \cdot \overline{B} \cdot \overline{C} \cdot \overline{D}$

Pin numbers shown are for DW, JT, and NT packages.

absolute maximum ratings over operating free-air temperature range†

Supply voltage, V_{CC}	-0.5 V to 7 V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$)	± 20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$)	± 20 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC})	± 25 mA
Continuous current through V_{CC} or GND pins	± 50 mA
Lead temperature 1,6 mm (1/16 in) from case for 60 s: FK or JT package	300°C
Lead temperature 1,6 mm (1/16 in) from case for 10 s: DW or NT package	260°C
Storage temperature range	-65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

		SN54HC7006			SN74HC7006			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	2	5	6	2	5	6	V
V_{IH}	High-level input voltage	$V_{CC} = 2$ V		1.5	$V_{CC} = 2$ V		1.5	V
		$V_{CC} = 4.5$ V		3.15	$V_{CC} = 4.5$ V		3.15	
		$V_{CC} = 6$ V		4.2	$V_{CC} = 6$ V		4.2	
V_{IL}	Low-level input voltage	$V_{CC} = 2$ V		0	$V_{CC} = 2$ V		0	V
		$V_{CC} = 4.5$ V		0	$V_{CC} = 4.5$ V		0	
		$V_{CC} = 6$ V		0	$V_{CC} = 6$ V		1.2	
V_I	Input voltage	0	V_{CC}		0	V_{CC}		V
V_O	Output voltage	0	V_{CC}		0	V_{CC}		V
t_t	Input transition (rise and fall) times	$V_{CC} = 2$ V		0	$V_{CC} = 2$ V		1000	ns
		$V_{CC} = 4.5$ V		0	$V_{CC} = 4.5$ V		500	
		$V_{CC} = 6$ V		0	$V_{CC} = 6$ V		400	
T_A	Operating free-air temperature	-55	125		-40	85		°C

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HC MOS Devices

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _{CC}	T _A = 25°C			SN54HC7006		SN74HC7006		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V _{OH}	V _I = V _{IH} or V _{IL} , I _{OH} = -20 μA	2 V	1.9	1.998		1.9		1.9	V	
		4.5 V	4.4	4.499		4.4		4.4		
		6 V	5.9	5.999		5.9		5.9		
	4.5 V	3.98	4.30		3.7		3.84			
V _{OL}	V _I = V _{IH} or V _{IL} , I _{OH} = -4 mA	2 V				0.1		0.1	V	
		4.5 V				0.001		0.1		
		6 V				0.001		0.1		
	4.5 V		0.17	0.26		0.4		0.33		
V _I	V _I = V _{IH} or V _{IL} , I _{OL} = 4 mA	2 V				0.15		0.26	V	
		4.5 V				0.15		0.26		
I _I	V _I = V _{CC} or 0, I _O = 0	2 V				±0.1		±100	nA	
		6 V				±0.1		±100		
I _{CC}	V _I = V _{CC} or 0, I _O = 0	6 V				2		40	μA	
C _i		2 to 6 V				3	10	10	pF	

switching characteristics over recommended operating free-air temperature range (unless otherwise noted), C_L = 50 pF (see Note 1)

NAND/NOR gates

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC}	T _A = 25°C			SN54HC7006		SN74HC7006		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t _{pd}	A, B, C or D	Y	2 V		45	90		135		115	ns
			4.5 V		9	18		27		23	
			6 V		8	15		23		20	
t _t		Y	2 V		38	75		110		95	ns
			4.5 V		8	15		22		19	
			6 V		6	13		19		16	

C _{pd}	Power dissipation capacitance per gate	No load, T _A = 25°C	20 pF typ
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inverters

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC}	T _A = 25°C			SN54HC7006		SN74HC7006		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t _{pd}	A	Y	2 V		45	95		145		120	ns
			4.5 V		9	19		29		24	
			6 V		8	16		25		20	
t _t		Y	2 V		38	75		110		95	ns
			4.5 V		8	15		22		19	
			6 V		6	13		19		16	

C _{pd}	Power dissipation capacitance per inverter	No load, T _A = 25°C	20 pF typ
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Note 1: Load circuits and voltage waveforms are shown in Section 1.