



# M74HC691

## 4 BIT BINARY COUNTER/REGISTER (3-STATE)

- HIGH SPEED:  
 $f_{MAX} = 53 \text{ MHz (TYP.) at } V_{CC} = 6V$
- LOW POWER DISSIPATION:  
 $I_{CC} = 4\mu A(\text{MAX.}) \text{ at } T_A=25^\circ C$
- HIGH NOISE IMMUNITY:  
 $V_{NIH} = V_{NIL} = 28 \% V_{CC} \text{ (MIN.)}$
- SYMMETRICAL OUTPUT IMPEDANCE:  
 $|I_{OH}| = I_{OL} = 6\text{mA (MIN) for } Q_A \text{ to } Q_D \text{ OUTPUT}$   
 $|I_{OH}| = I_{OL} = 4\text{mA (MIN) for RCO OUTPUT}$
- BALANCED PROPAGATION DELAYS:  
 $t_{PLH} \cong t_{PHL}$
- WIDE OPERATING VOLTAGE RANGE:  
 $V_{CC} \text{ (OPR)} = 2V \text{ to } 6V$
- PIN AND FUNCTION COMPATIBLE WITH  
 74 SERIES 691



### ORDER CODES

PACKAGE	TUBE	T & R
DIP	M74HC691B1R	
SOP	M74HC691M1R	M74HC691RM13TR
TSSOP		M74HC691TTR

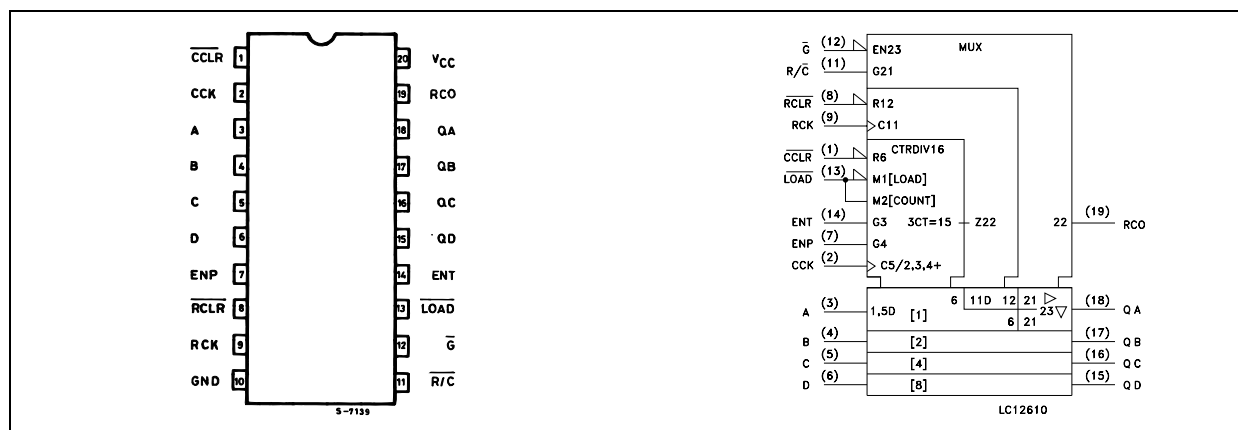
### DESCRIPTION

The M74HC691 is an high speed CMOS DECADE/COUNTER REGISTER (3 STATE) fabricated with silicon gate C<sup>2</sup>MOS technology. The internal circuit is composed of 3 stages including buffer output, which offers high noise immunity and stable output. This device incorporates a synchronous counter, four bit D-type register, and quadruple two-line to one-line multiplexers with three-state outputs in a single 20 pin package. The counter can be programmed from the data inputs and have enable P and enable T inputs and a ripple carry output for easy expansion. The register/counter select input, R/C, selects the counter when low or the register when high for the three state-outputs, QA, QB, QC, and

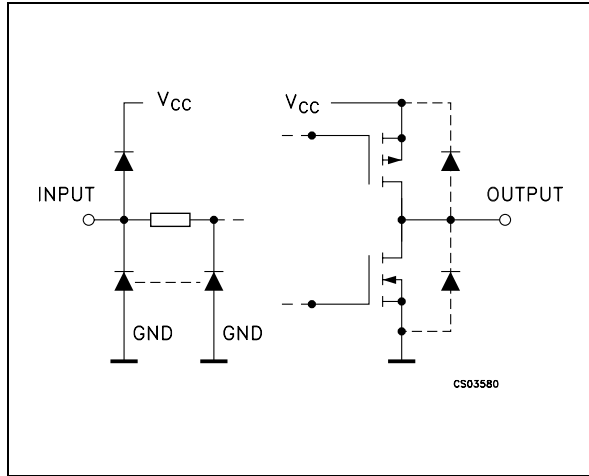
QD. If the LOAD input ( $\overline{\text{LOAD}}$ ) is held "L" DATA input (A - D) are loaded into the internal counter at positive edge of counter clock input (CCK). In the counter mode, internal counter counts up at the positive of the counter clock. If the counter clear inputs ( $\overline{\text{CCLR}}$ ) is held "L", the internal counter is cleared asynchronously to the counter clock. The internal counter's outputs are stored in the output register at the positive edge of the register clock (RCK). If the register clear input (RCLR) is held "L" the register is cleared asynchronously to register clock.

All inputs are equipped with protection circuits against static discharge and transient excess voltage.

### PIN CONNECTION AND IEC LOGIC SYMBOLS



INPUT AND OUTPUT EQUIVALENT CIRCUIT



PIN DESCRIPTION

PIN No	SYMBOL	NAME AND FUNCTION
3 to 6	A to D	Data Inputs
7, 14	ENT, ENP	Enable Inputs
15 to 18	QA to QD	Data Outputs
1	CCLR	Counter Clear (Active LOW)
2	CCK	Counter Clock
11	R/C	Counter/Register Select
8	RCLR	Register Clear (Active LOW)
9	RCK	Register Clock
19	RCO	Ripple Counter Output
10	GND	Ground (0V)
20	V <sub>CC</sub>	Positive Supply Voltage

TRUTH TABLE

INPUTS									OUTPUTS				FUNCTION
CCLR	LOAD	ENP	ENT	CCK	RCLR	RCK	R/C	G	QA	QB	QC	QD	
X	X	X	X	X	X	X	X	X	Z	Z	Z	Z	HIGH IMPEDANCE
L	X	X	X	X	X	X	L	L	L	L	L	L	CLEAR COUNTER
H	L	X	X	□	X	X	L	L	a	b	c	d	LOAD COUNTER
H	H	L	X	□	X	X	L	L	NO CHANGE				NO COUNT
H	H	X	L	□	X	X	L	L	NO CHANGE				NO COUNT
H	H	H	H	□	X	X	L	L	COUNT UP				COUNT UP
H	X	X	X	□	X	X	L	L	NO CHANGE				NO COUNT
X	X	X	X	X	L	X	H	L	L	L	L	L	CLEAR REGISTER
X	X	X	X	X	H	□	H	L	a'	b'	c'	d'	LOAD REGISTER
X	X	X	X	X	H	□	H	L	NO CHANGE				NO LOAD

X : Don't Care

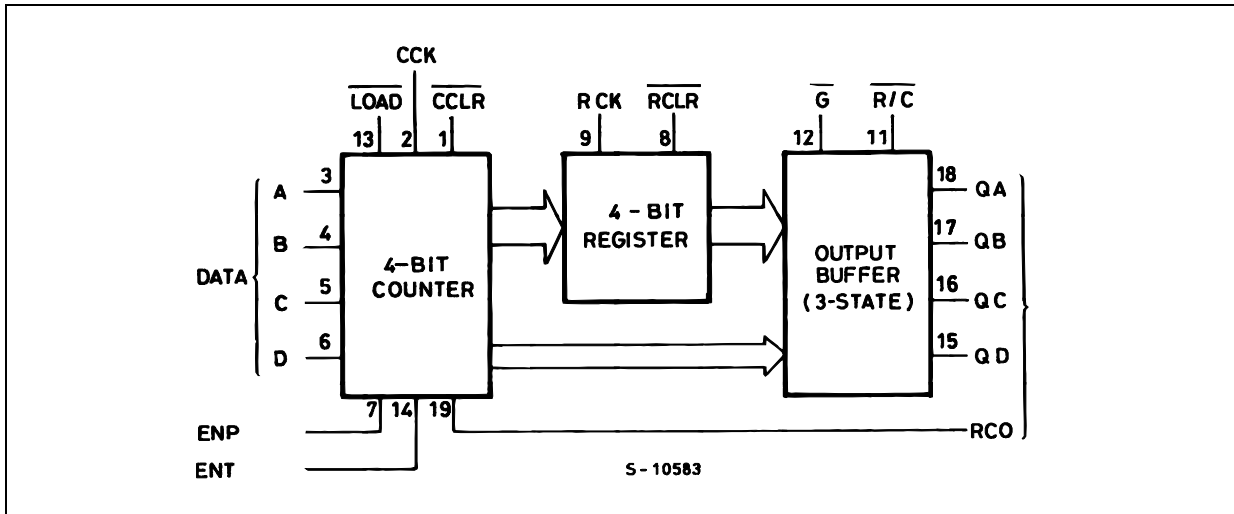
Z : High Impedance

a-d : The level of steady state inputs at inputs A through D respectively.

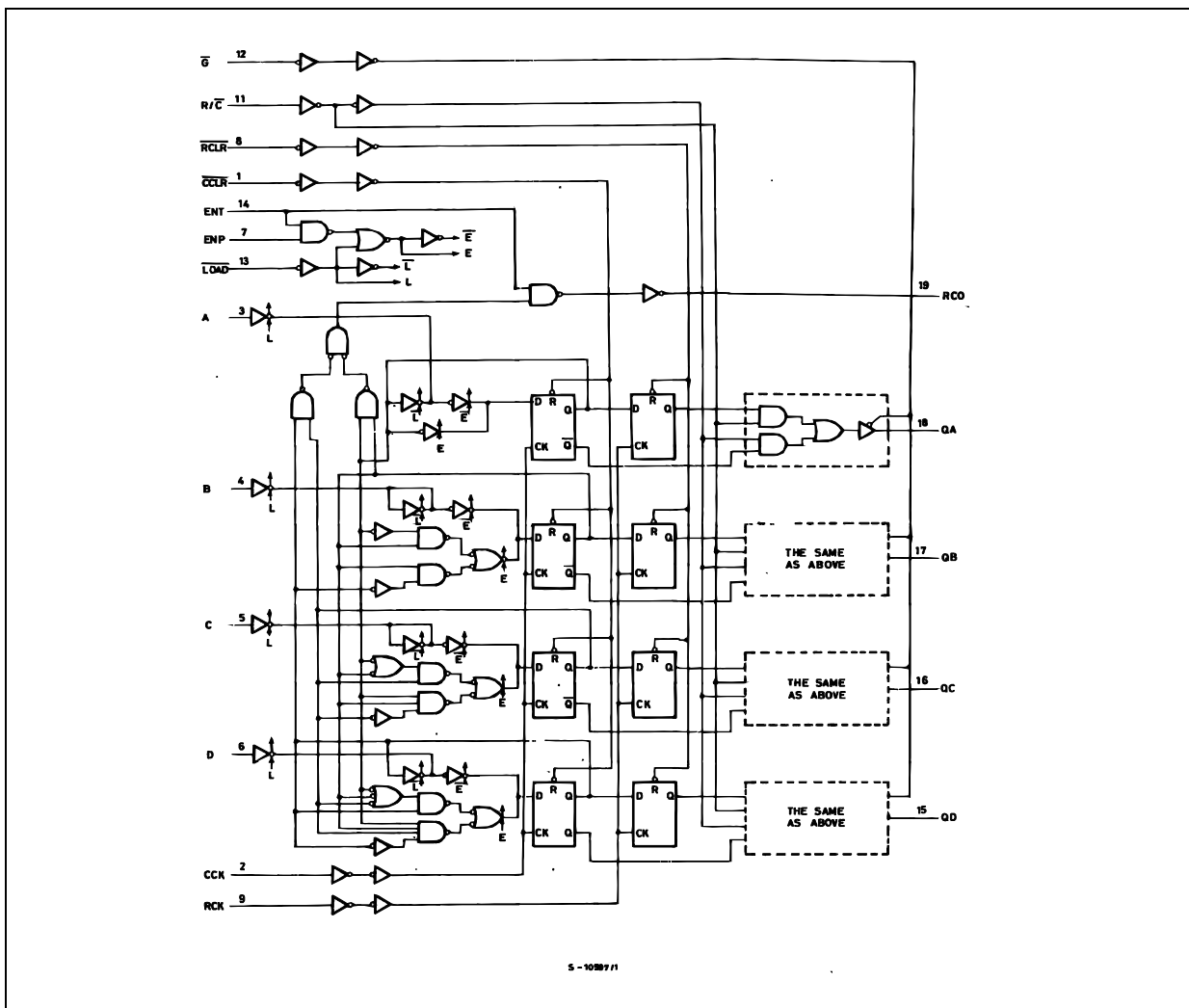
a'-d' : The level of steady state outputs at internal counter outputs a' through qd' respectively

RCO = QA · QB · QC · QD · ENT

BLOCK DIAGRAM



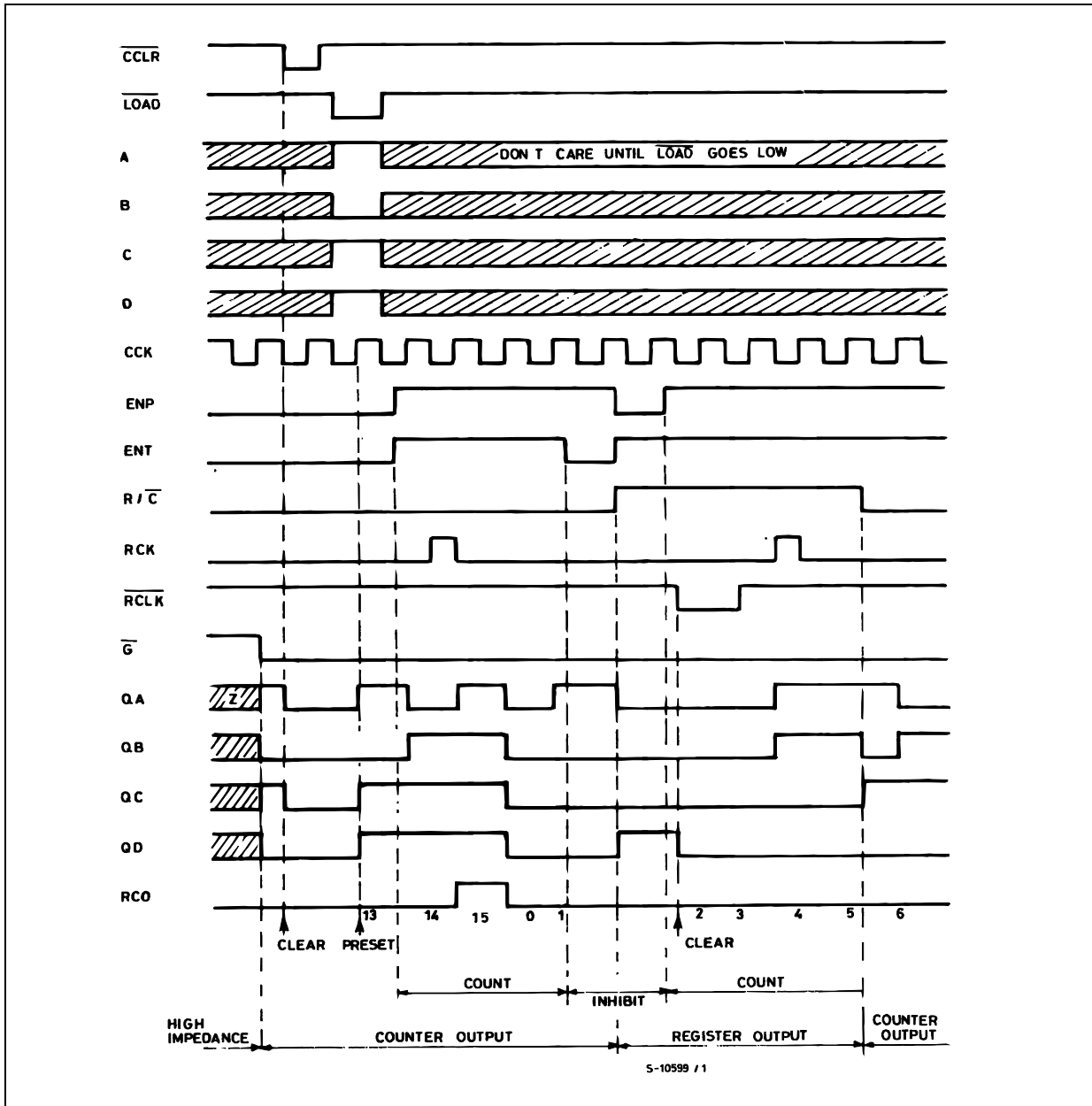
LOGIC DIAGRAM



This logic diagram has not been used to estimate propagation delays



TIMING CHART



**ABSOLUTE MAXIMUM RATINGS**

Symbol	Parameter	Value	Unit
$V_{CC}$	Supply Voltage	-0.5 to +7	V
$V_I$	DC Input Voltage	-0.5 to $V_{CC} + 0.5$	V
$V_O$	DC Output Voltage	-0.5 to $V_{CC} + 0.5$	V
$I_{IK}$	DC Input Diode Current	$\pm 20$	mA
$I_{OK}$	DC Output Diode Current	$\pm 20$	mA
$I_O$	DC Output Source Sink Current per Output PIN (RCO) (QA to QD)	$\pm 25$ $\pm 35$	mA
$I_{CC}$ or $I_{GND}$	DC $V_{CC}$ or Ground Current	$\pm 70$	mA
$P_D$	Power Dissipation	500(*)	mW
$T_{stg}$	Storage Temperature	-65 to +150	°C
$T_L$	Lead Temperature (10 sec)	300	°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied

(\*) 500mW at 65 °C; derate to 300mW by 10mW/°C from 65°C to 85°C

**RECOMMENDED OPERATING CONDITIONS**

Symbol	Parameter	Value	Unit	
$V_{CC}$	Supply Voltage	2 to 6	V	
$V_I$	Input Voltage	0 to $V_{CC}$	V	
$V_O$	Output Voltage	0 to $V_{CC}$	V	
$T_{op}$	Operating Temperature	-55 to 125	°C	
$t_r, t_f$	Input Rise and Fall Time	$V_{CC} = 2.0V$	0 to 1000	ns
		$V_{CC} = 4.5V$	0 to 500	ns
		$V_{CC} = 6.0V$	0 to 400	ns

## DC SPECIFICATIONS

Symbol	Parameter	Test Condition		Value						Unit	
		V <sub>CC</sub> (V)		T <sub>A</sub> = 25°C			-40 to 85°C		-55 to 125°C		
				Min.	Typ.	Max.	Min.	Max.	Min.		Max.
V <sub>IH</sub>	High Level Input Voltage	2.0		1.5			1.5		1.5		V
		4.5		3.15			3.15		3.15		
		6.0		4.2			4.2		4.2		
V <sub>IL</sub>	Low Level Input Voltage	2.0				0.5		0.5		0.5	V
		4.5				1.35		1.35		1.35	
		6.0				1.8		1.8		1.8	
V <sub>OH</sub>	High Level Output Voltage (QA - QD)	2.0	I <sub>O</sub> =-20 μA	1.9	2.0		1.9		1.9		V
		4.5	I <sub>O</sub> =-20 μA	4.4	4.5		4.4		4.4		
		6.0	I <sub>O</sub> =-20 μA	5.9	6.0		5.9		5.9		
		4.5	I <sub>O</sub> =-6.0 mA	4.18	4.31		4.13		4.10		
		6.0	I <sub>O</sub> =-7.8 mA	5.68	5.8		5.63		5.60		
V <sub>OH</sub>	High Level Output Voltage (RCO)	2.0	I <sub>O</sub> =-20 μA	1.9	2.0		1.9		1.9		V
		4.5	I <sub>O</sub> =-20 μA	4.4	4.5		4.4		4.4		
		6.0	I <sub>O</sub> =-20 μA	5.9	6.0		5.9		5.9		
		4.5	I <sub>O</sub> =-4.0 mA	4.18	4.31		4.13		4.10		
		6.0	I <sub>O</sub> =-5.2 mA	5.68	5.8		5.63		5.60		
V <sub>OL</sub>	Low Level Output Voltage (QA - QD)	2.0	I <sub>O</sub> =20 μA		0.0	0.1		0.1		0.1	V
		4.5	I <sub>O</sub> =20 μA		0.0	0.1		0.1		0.1	
		6.0	I <sub>O</sub> =20 μA		0.0	0.1		0.1		0.1	
		4.5	I <sub>O</sub> =6.0 mA		0.17	0.26		0.37		0.40	
		6.0	I <sub>O</sub> =7.8 mA		0.18	0.26		0.37		0.40	
V <sub>OL</sub>	Low Level Output Voltage (RCO)	2.0	I <sub>O</sub> =20 μA		0.0	0.1		0.1		0.1	V
		4.5	I <sub>O</sub> =20 μA		0.0	0.1		0.1		0.1	
		6.0	I <sub>O</sub> =20 μA		0.0	0.1		0.1		0.1	
		4.5	I <sub>O</sub> =4.0 mA		0.17	0.26		0.37		0.40	
		6.0	I <sub>O</sub> =5.2 mA		0.18	0.26		0.37		0.40	
I <sub>I</sub>	Input Leakage Current	6.0	V <sub>I</sub> = V <sub>CC</sub> or GND			± 0.1		± 1		± 1	μA
I <sub>OZ</sub>	High Impedance Output Leakage Current	6.0	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> V <sub>O</sub> = V <sub>CC</sub> or GND			± 0.5		± 5		± 10	μA
I <sub>CC</sub>	Quiescent Supply Current	6.0	V <sub>I</sub> = V <sub>CC</sub> or GND			4		40		80	μA

AC ELECTRICAL CHARACTERISTICS ( $C_L = 50 \text{ pF}$ , Input  $t_r = t_f = 6 \text{ ns}$ )

Symbol	Parameter	Test Condition			Value						Unit	
		$V_{CC}$ (V)	$C_L$ (pF)		$T_A = 25^\circ\text{C}$			$-40 \text{ to } 85^\circ\text{C}$		$-55 \text{ to } 125^\circ\text{C}$		
					Min.	Typ.	Max.	Min.	Max.	Min.		Max.
$t_{TLH} \ t_{THL}$	Output Transition Time (Q)	2.0	50			25	60		75		90	ns
		4.5			7	12		15		19		
		6.0			6	10		13		15		
$t_{TLH} \ t_{THL}$	Output Transition Time (RCO)	2.0	50			30	75		95		115	ns
		4.5			8	15		19		23		
		6.0			7	13		16		20		
$t_{PLH} \ t_{PHL}$	Propagation Delay Time (CCK - Q)	2.0	50			82	205		255		310	ns
		4.5			26	41		51		62		
		6.0			22	35		43		53		
		2.0	150			95	235		295		255	
		4.5			30	47		59		71		
6.0		26	40		50		60					
$t_{PLH} \ t_{PHL}$	Propagation Delay Time (RCK - Q)	2.0	50			86	210		265		315	ns
		4.5			27	42		53		63		
		6.0			23	36		45		54		
		2.0	150			99	240		300		360	
		4.5			31	48		60		72		
6.0		26	41		51		61					
$t_{PLH} \ t_{PHL}$	Propagation Delay Time (CCK - RCO)	2.0	50			65	165		205		250	ns
		4.5			21	33		41		50		
		6.0			18	28		35		43		
$t_{PLH} \ t_{PHL}$	Propagation Delay Time (R/C - Q)	2.0	50			59	145		180		220	ns
		4.5			18	29		36		44		
		6.0			15	25		31		37		
		2.0	150			72	175		220		265	
		4.5			22	35		44		53		
6.0		19	30		37		45					
$t_{PLH} \ t_{PHL}$	Propagation Delay Time (ENT - RCO)	2.0	50			36	100		125		150	ns
		4.5			12	20		25		30		
		6.0			10	17		21		26		
$t_{PHL}$	Propagation Delay Time (CCLR - Q)	2.0	50			91	225		280		340	ns
		4.5			29	45		56		68		
		6.0			25	38		48		58		
		2.0	150			104	255		320		385	
		4.5			33	51		64		77		
6.0		28	43		54		65					
$t_{PHL}$	Propagation Delay Time (RCLR - Q)	2.0	50			86	210		265		315	ns
		4.5			27	42		53		63		
		6.0			23	36		45		54		
		2.0	150			100	240		300		360	
		4.5			31	48		60		72		
6.0		26	41		51		61					
$t_{PHL}$	Propagation Delay Time (CCLR - RCO)	2.0	50			70	175		220		265	ns
		4.5			22	35		44		53		
		6.0			19	30		37		45		

## M74HC691

Symbol	Parameter	Test Condition			Value						Unit	
		V <sub>CC</sub> (V)	C <sub>L</sub> (pF)		T <sub>A</sub> = 25°C			-40 to 85°C		-55 to 125°C		
					Min.	Typ.	Max.	Min.	Max.	Min.		Max.
f <sub>MAX</sub>	Maximum Clock Frequency	2.0	50		4.4	12		3.6		3		MHz
		4.5			22	45		18		15		
		6.0			26	53		21		18		
t <sub>PZL</sub> t <sub>PZH</sub>	High Impedance Output Enable Time	2.0	50	R <sub>L</sub> = 1 KΩ		48	120		150		180	ns
		4.5				15	24		30		36	
		6.0				13	20		26		31	
		2.0	150	R <sub>L</sub> = 1 KΩ		61	150		190		225	ns
		4.5				19	30		38		45	
		6.0				17	26		32		38	
t <sub>PLZ</sub> t <sub>PHZ</sub>	High Impedance Output Disable Time	2.0	50	R <sub>L</sub> = 1 KΩ		32	145		180		220	ns
		4.5				15	29		36		44	
		6.0				13	25		31		37	
t <sub>W(L)</sub> t <sub>W(H)</sub>	Minimum Pulse Width (CCK, RCK)	2.0	50			28	75		95		110	ns
		4.5				7	15		19		22	
		6.0				6	13		16		19	
t <sub>W(L)</sub>	Minimum Pulse Width (CCLR - RCLR)	2.0	50			40	75		95		110	ns
		4.5				8	15		19		22	
		6.0				7	13		16		19	
t <sub>s</sub>	Minimum Set-up Time (LOAD, ENT, ENP)	2.0	50			68	150		190		220	ns
		4.5				17	30		38		44	
		6.0				14	26		32		37	
t <sub>s</sub>	Minimum Set-up Time (A, B, C, D)	2.0	50			44	100		125		145	ns
		4.5				11	20		25		29	
		6.0				9	17		21		25	
t <sub>s</sub>	Minimum Set-up Time (CCK - RCK)	2.0	50			48	125		155		180	ns
		4.5				12	25		31		36	
		6.0				10	21		26		31	
t <sub>h</sub>	Minimum Hold Time	2.0	50				0		0		0	ns
		4.5					0		0		0	
		6.0					0		0		0	
t <sub>REM</sub>	Minimum Removal Time	2.0	50				25		30		40	ns
		4.5					5		6		8	
		6.0					5		5		7	

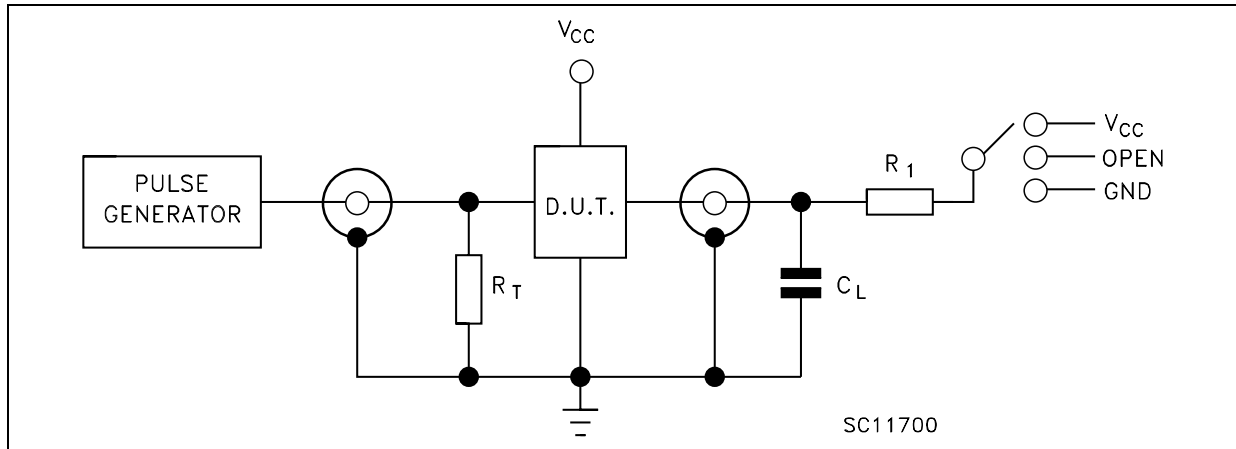
### CAPACITIVE CHARACTERISTICS

Symbol	Parameter	Test Condition			Value						Unit	
		V <sub>CC</sub> (V)			T <sub>A</sub> = 25°C			-40 to 85°C		-55 to 125°C		
					Min.	Typ.	Max.	Min.	Max.	Min.		Max.
C <sub>IN</sub>	Input Capacitance					5	10		10		10	pF
C <sub>PD</sub>	Power Dissipation Capacitance (note 1)					70						pF

1) C<sub>PD</sub> is defined as the value of the IC's internal equivalent capacitance which is calculated from the operating current consumption without load. (Refer to Test Circuit). Average operating current can be obtained by the following equation.  $I_{CC(oper)} = C_{PD} \times V_{CC} \times f_{IN} + I_{CC}$



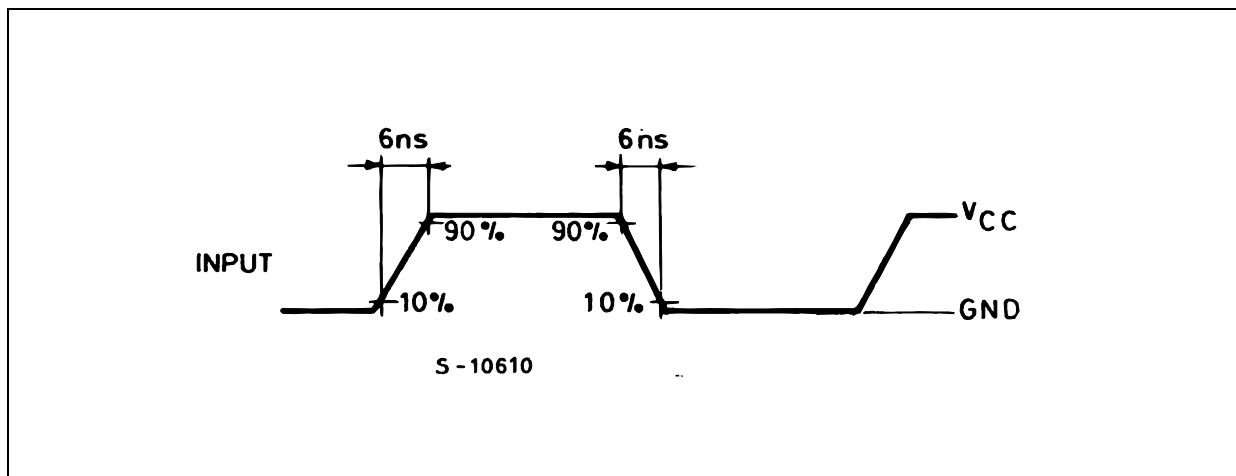
TEST CIRCUIT



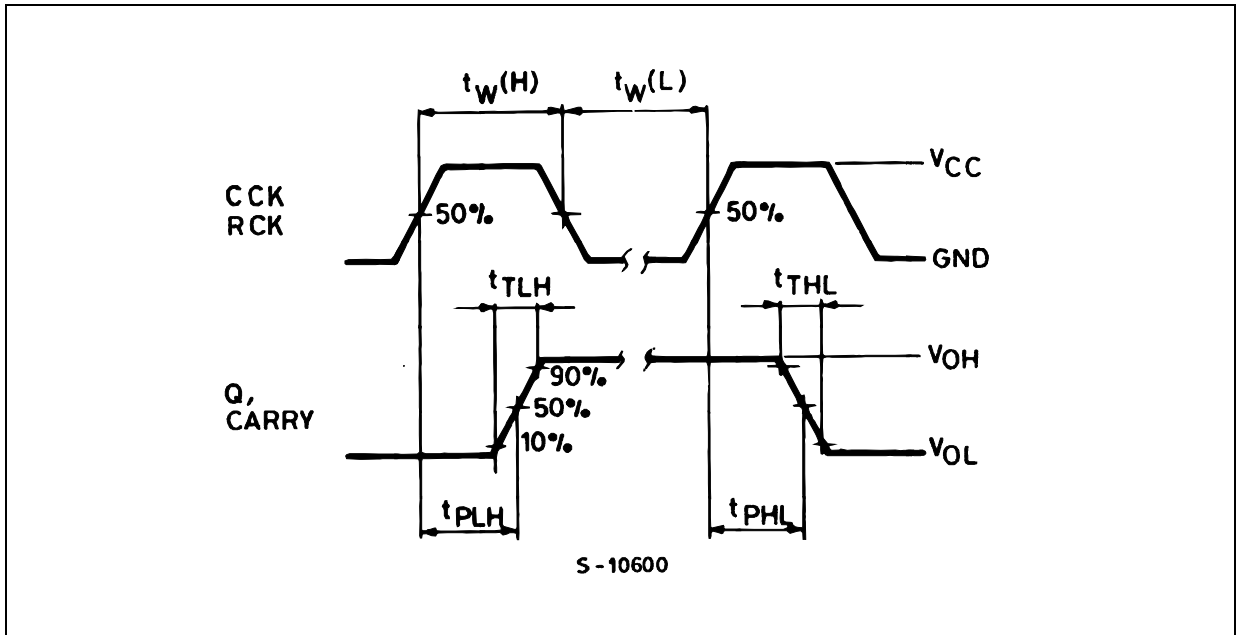
TEST	SWITCH
$t_{PLH}, t_{PHL}$	Open
$t_{PZL}, t_{PLZ}$	$V_{CC}$
$t_{PZH}, t_{PHZ}$	GND

$C_L = 50\text{pF}/150\text{pF}$  or equivalent (includes jig and probe capacitance)  
 $R_1 = 1\text{K}\Omega$  or equivalent  
 $R_T = Z_{OUT}$  of pulse generator (typically  $50\Omega$ )

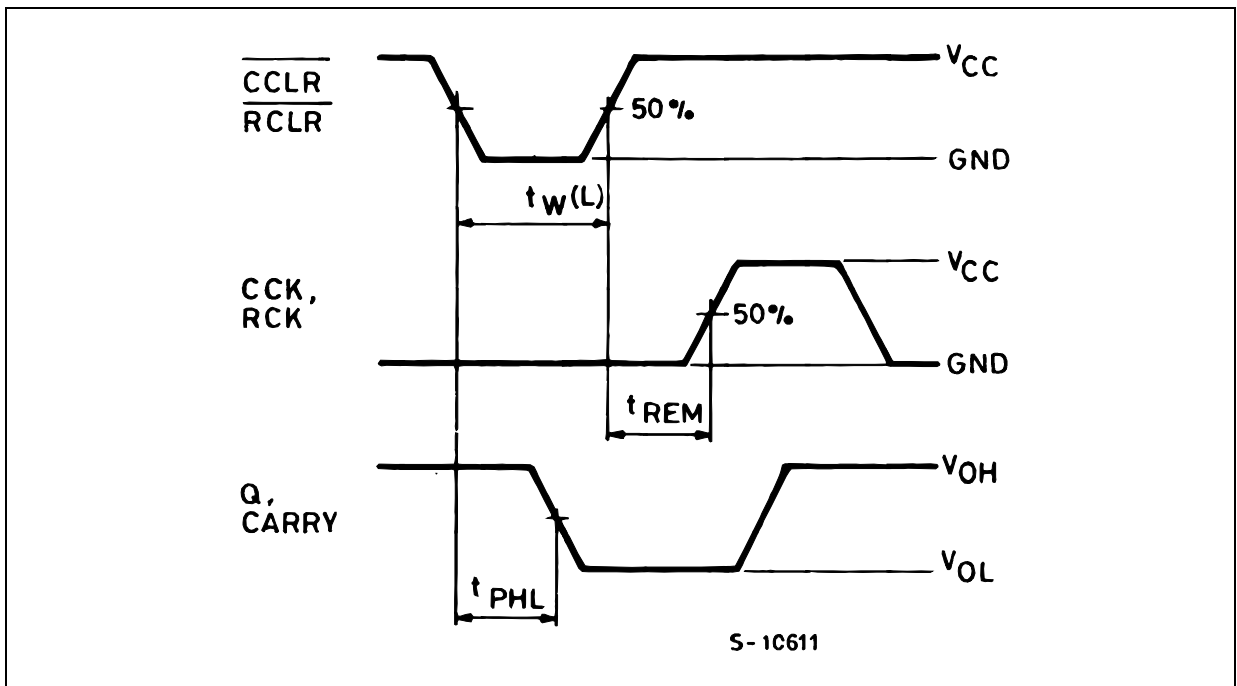
WAVEFORM 1: INPUT WAVEFORM ( $f=1\text{MHz}$ ; 50% duty cycle)



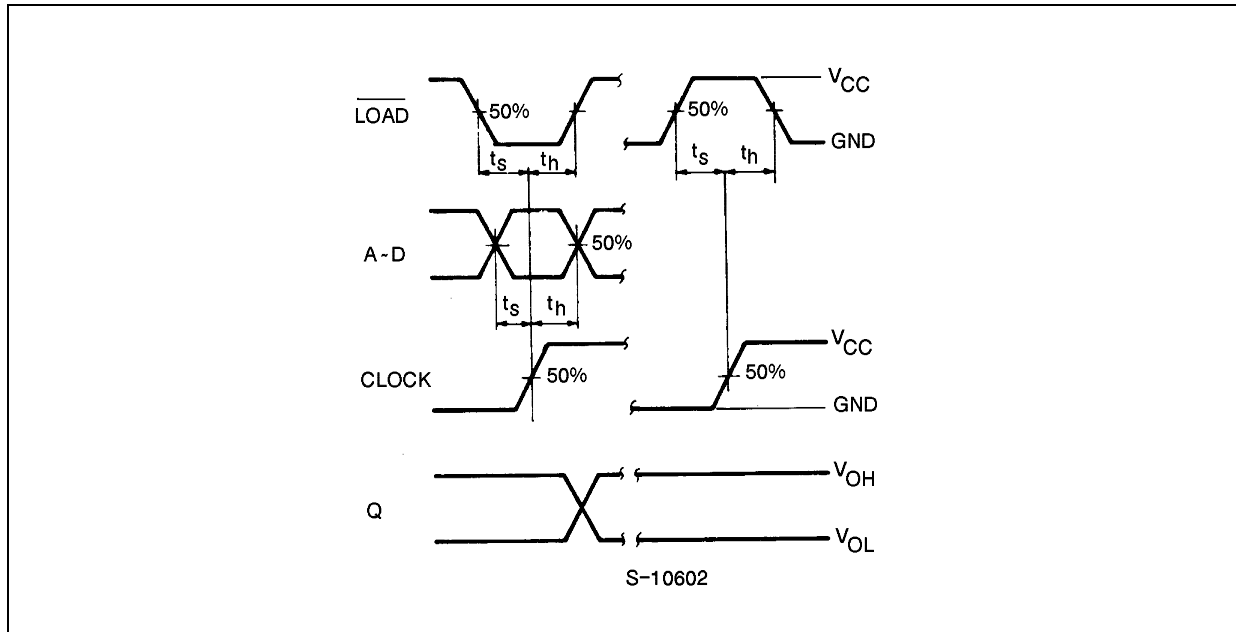
WAVEFORM 2 : MINIMUM PULSE WIDTH, PROPAGATION DELAY TIME (f=1MHz; 50% duty cycle)



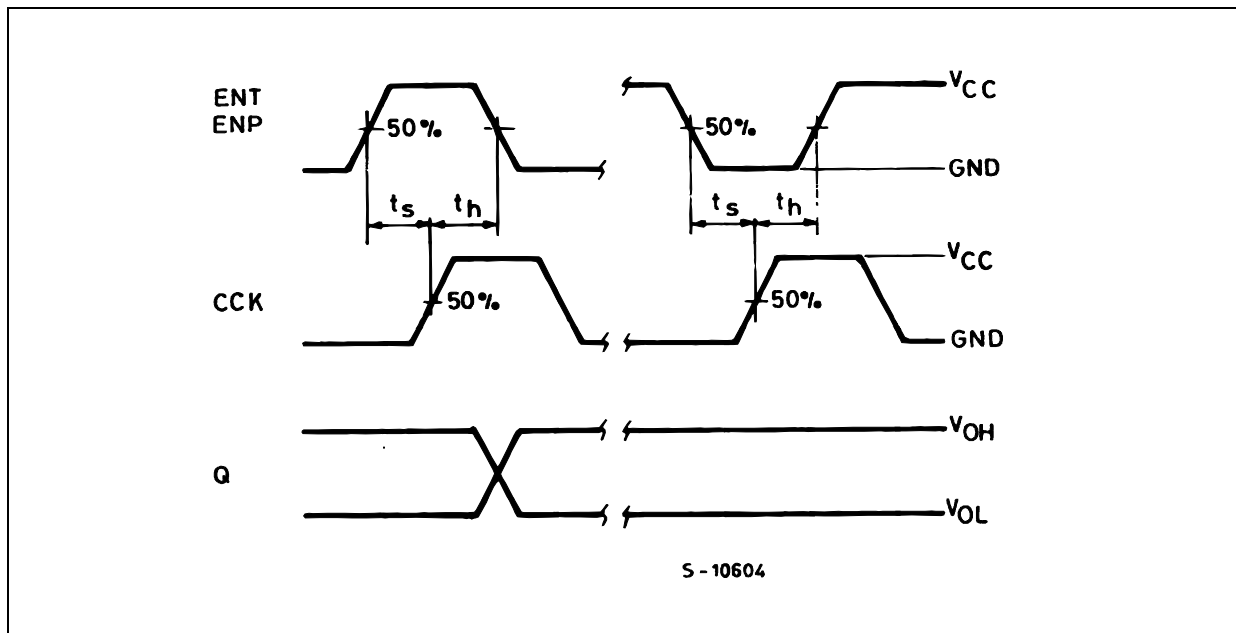
WAVEFORM 3 : MINIMUM PULSE WIDTH AND REMOVAL TIME (f=1MHz; 50% duty cycle)



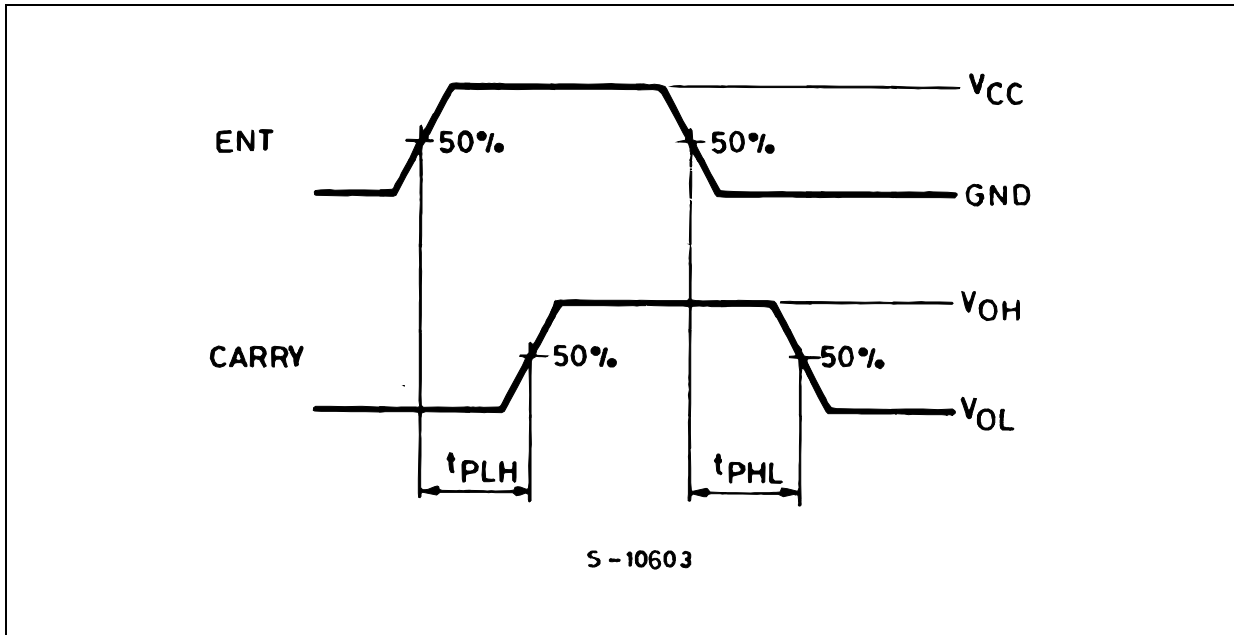
WAVEFORM 4 : MINIMUM SETUP AND HOLD TIME (f=1MHz; 50% duty cycle)



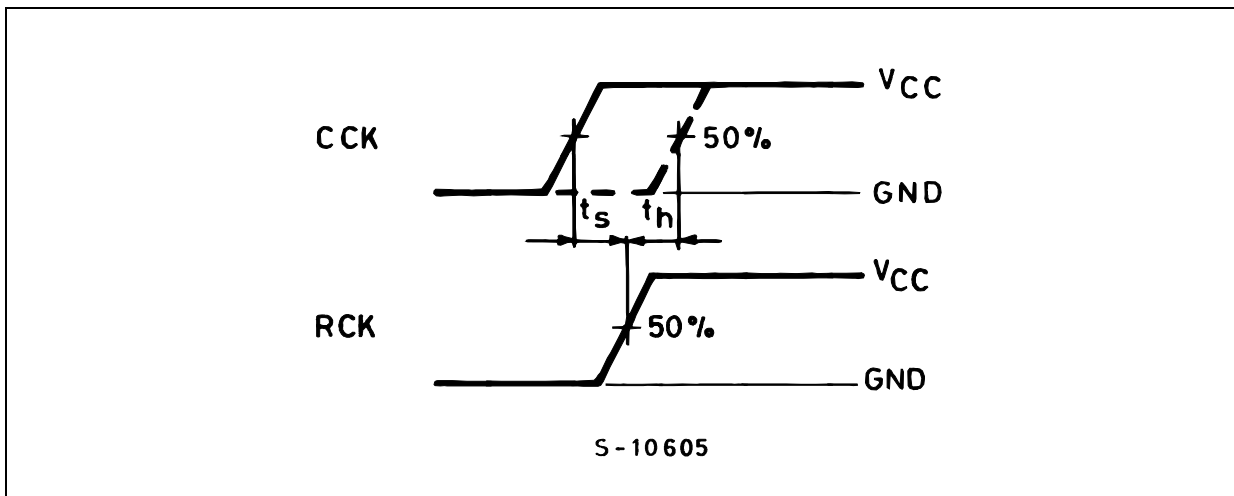
WAVEFORM 5 : MINIMUM SETUP AND HOLD TIME (f=1MHz; 50% duty cycle)



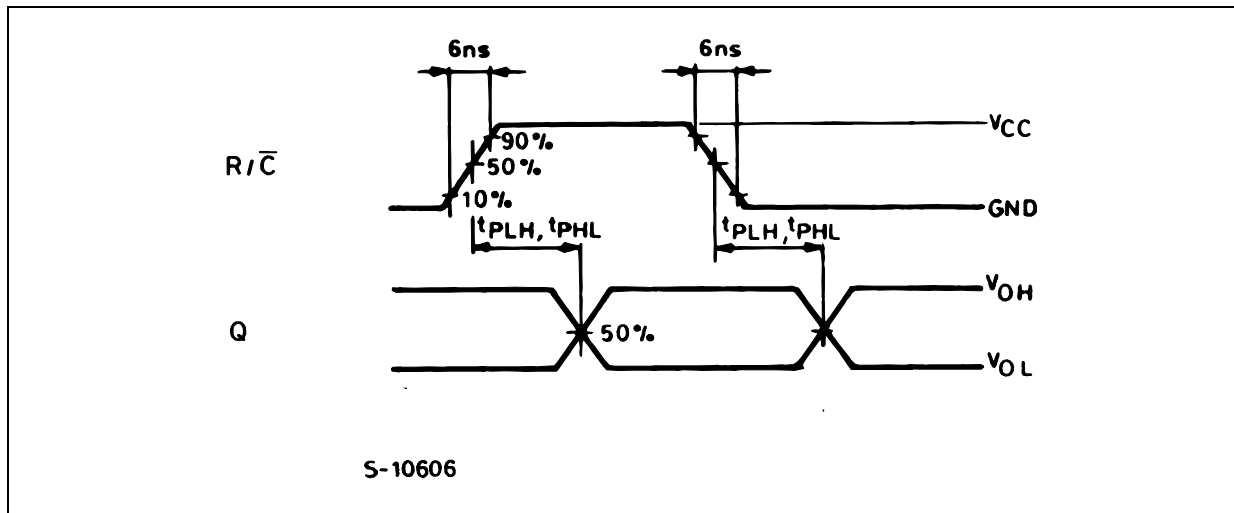
WAVEFORM 6 : PROPAGATION DELAY TIME (f=1MHz; 50% duty cycle)



WAVEFORM 7 : MINIMUM SETUP AND HOLD TIME (f=1MHz; 50% duty cycle)



WAVEFORM 8 : PROPAGATION DELAY TIME (f=1MHz; 50% duty cycle)



$t_{PLZ}$ ,  $t_{PZL}$

The  $1K\Omega$  load resistors should be connected between outputs and  $V_{CC}$  line and the  $50pF$  load capacitor should be connected between outputs and GND line.

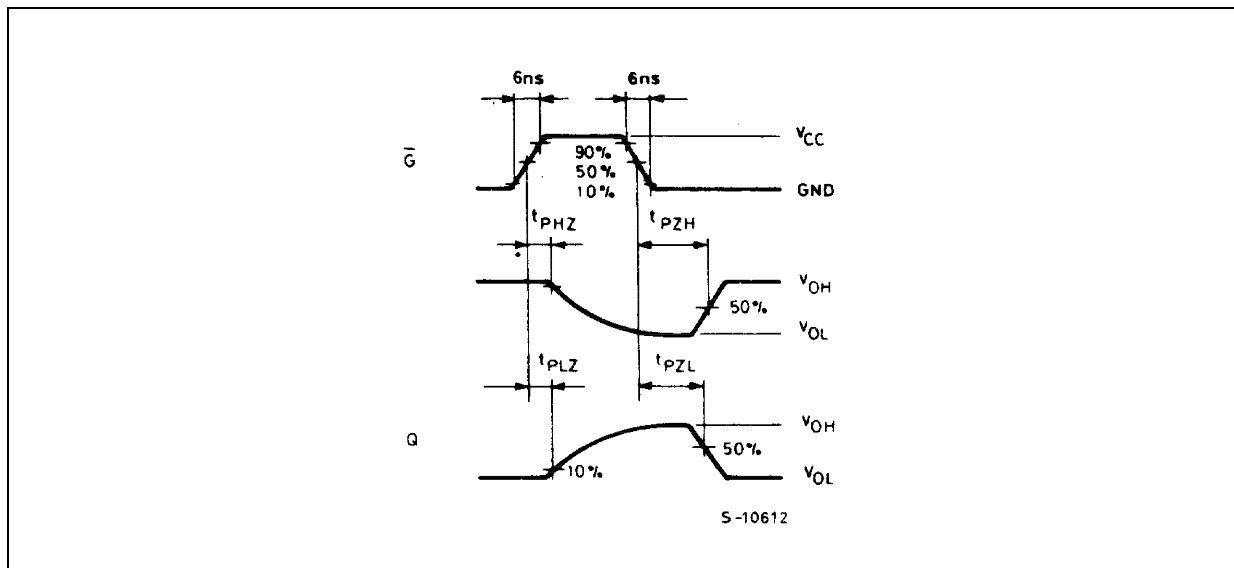
All inputs except  $\bar{G}$  input should be connected to  $V_{CC}$  or GND line such that outputs will be in low logic level while  $\bar{G}$  input is held low.

$t_{PHZ}$ ,  $t_{PZH}$

The  $1K\Omega$  load resistors and the  $50pF$  load capacitors should be connected between each output and GND line.

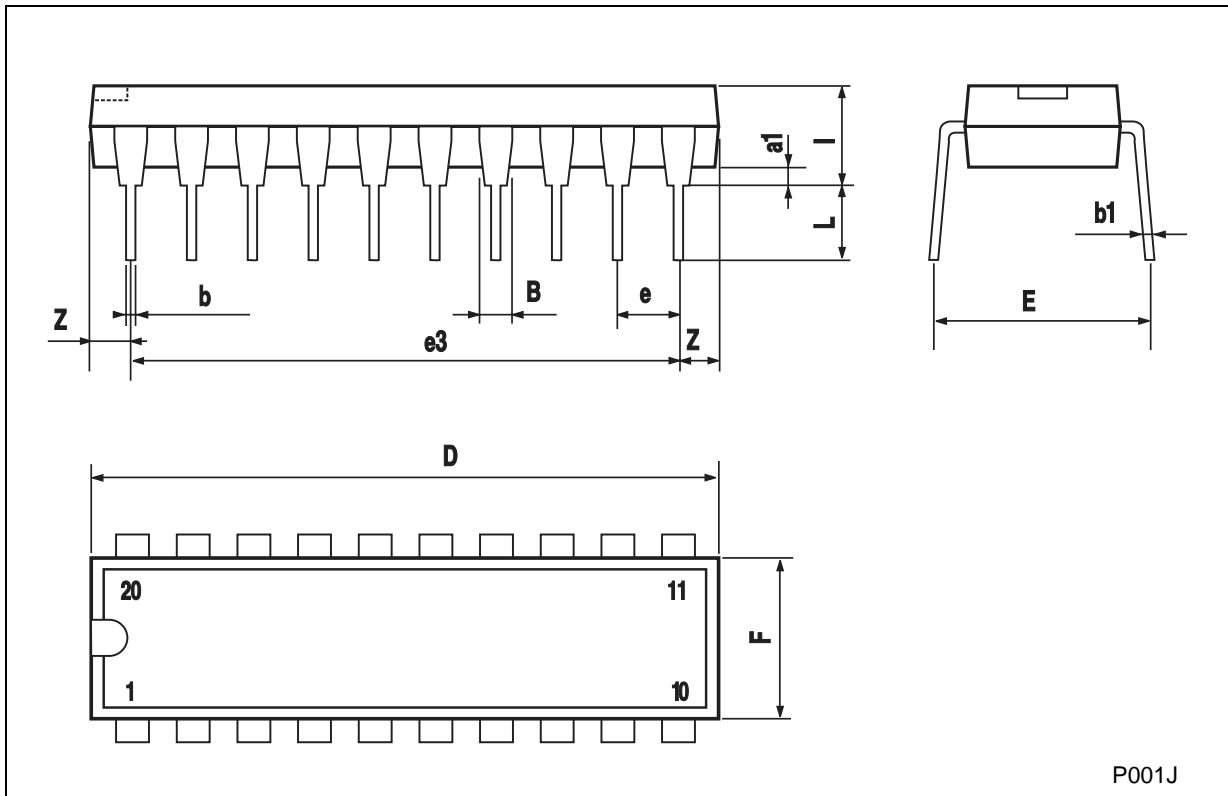
All inputs except  $\bar{G}$  input should be connected to  $V_{CC}$  or GND line such that outputs will be in low logic level while  $\bar{G}$  input is held low.

WAVEFORM 9 : OUTPUT ENABLE AND DISABLE TIME (f=1MHz; 50% duty cycle)



**Plastic DIP-20 (0.25) MECHANICAL DATA**

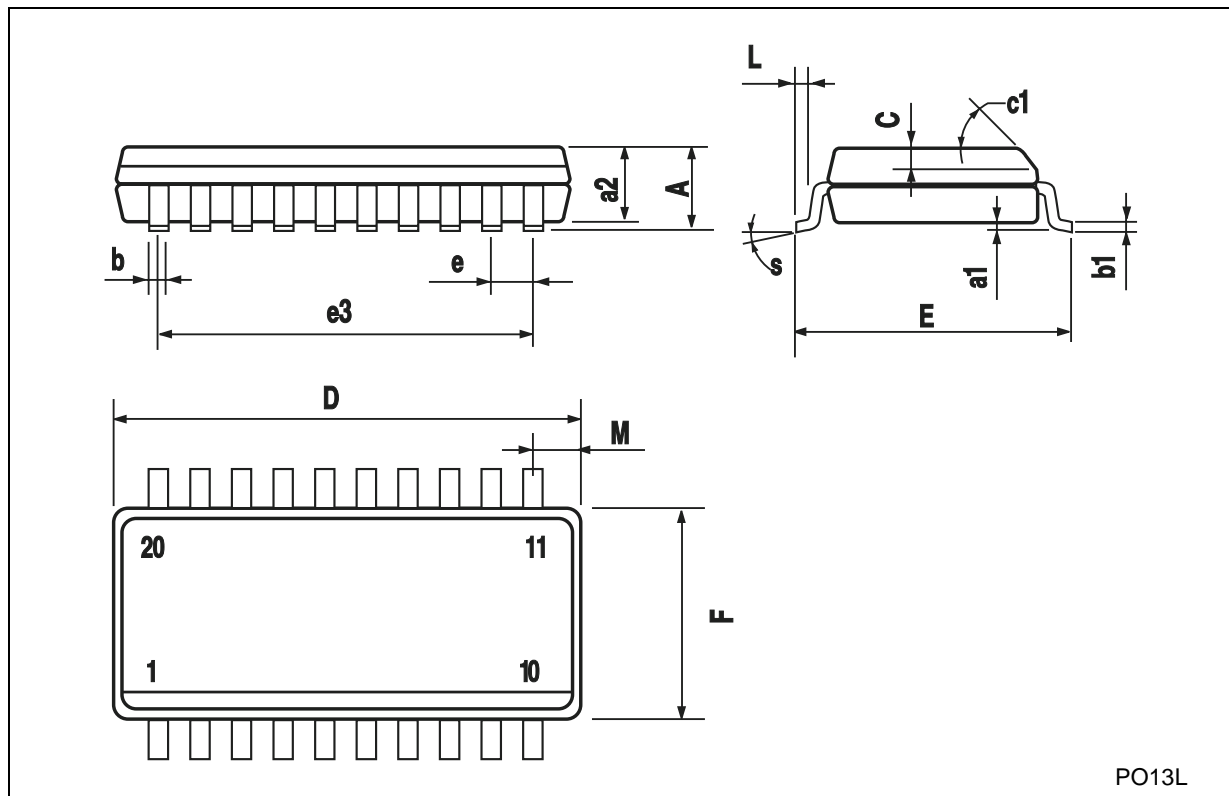
DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
a1	0.254			0.010		
B	1.39		1.65	0.055		0.065
b		0.45			0.018	
b1		0.25			0.010	
D			25.4			1.000
E		8.5			0.335	
e		2.54			0.100	
e3		22.86			0.900	
F			7.1			0.280
I			3.93			0.155
L		3.3			0.130	
Z			1.34			0.053



P001J

## SO-20 MECHANICAL DATA

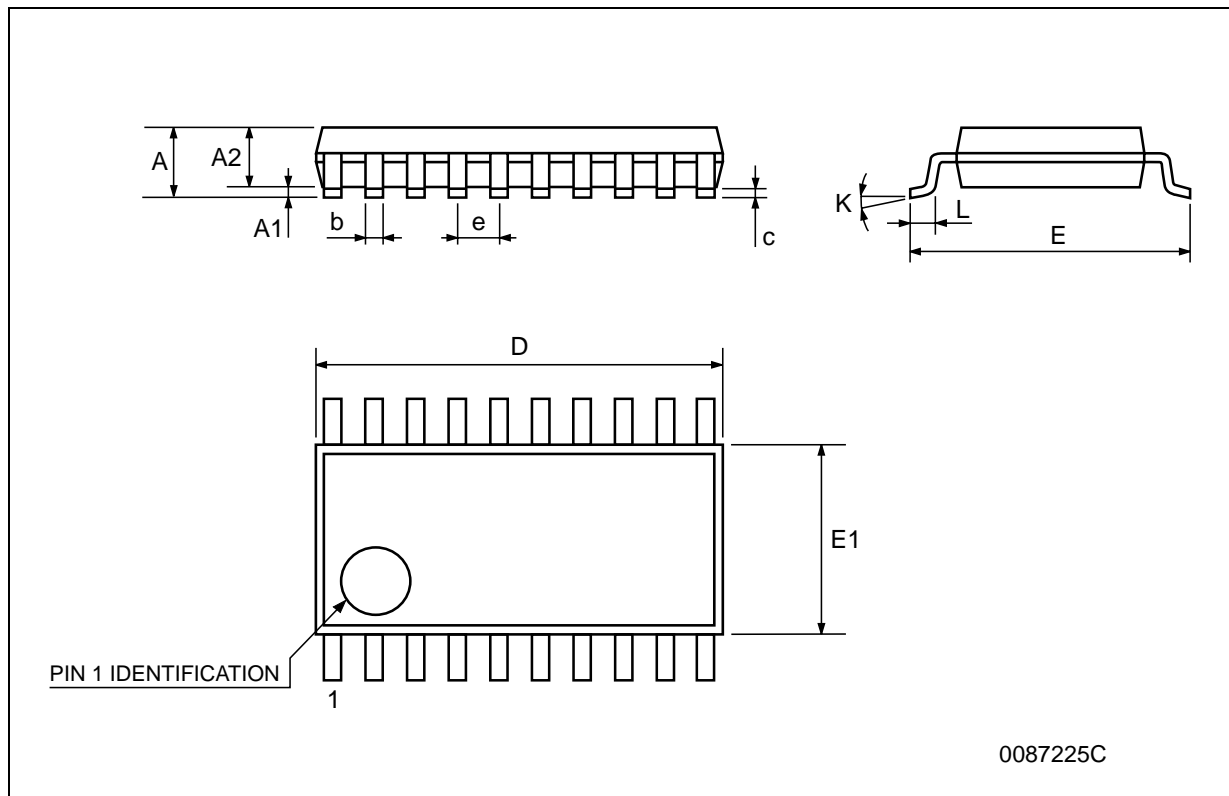
DIM.	mm.			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			2.65			0.104
a1	0.1		0.2	0.004		0.008
a2			2.45			0.096
b	0.35		0.49	0.014		0.019
b1	0.23		0.32	0.009		0.012
C		0.5			0.020	
c1	45° (typ.)					
D	12.60		13.00	0.496		0.512
E	10.00		10.65	0.393		0.419
e		1.27			0.050	
e3		11.43			0.450	
F	7.40		7.60	0.291		0.300
L	0.50		1.27	0.020		0.050
M			0.75			0.029
S	8° (max.)					



PO13L

**TSSOP20 MECHANICAL DATA**

DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A			1.2			0.047
A1	0.05		0.15	0.002	0.004	0.006
A2	0.8	1	1.05	0.031	0.039	0.041
b	0.19		0.30	0.007		0.012
c	0.09		0.20	0.004		0.0089
D	6.4	6.5	6.6	0.252	0.256	0.260
E	6.2	6.4	6.6	0.244	0.252	0.260
E1	4.3	4.4	4.48	0.169	0.173	0.176
e		0.65 BSC			0.0256 BSC	
K	0°		8°	0°		8°
L	0.45	0.60	0.75	0.018	0.024	0.030





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