

MM54HC534/MM74HC534 TRI-STATE® Octal D-Type Flip-Flop with Inverted Outputs

General Description

These high speed Octal D-Type Flip-Flops utilize advanced silicon-gate CMOS technology. They possess the high noise immunity and low power consumption of standard CMOS integrated circuits, as well as the ability to drive 15 LS-TTL loads. Due to the large output drive capability and the TRI-STATE feature, these devices are ideally suited for interfacing with bus lines in a bus organized system.

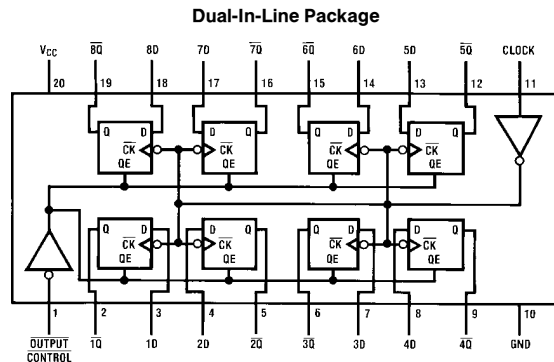
These devices are positive edge triggered flip-flops. Data at the D inputs, meeting the setup and hold time requirements, are inverted and transferred to the \bar{Q} outputs on positive going transitions of the CLOCK (CK) input. When a high logic level is applied to the OUTPUT CONTROL (OC) input, all outputs go to a high impedance state, regardless of what signals are present at the other inputs and the state of the storage elements.

The 54HC/74HC logic family is speed, function, and pinout compatible with the standard 54LS/74LS logic family. All inputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

Features

- Typical propagation delay: 23 ns
- Wide operating voltage range: 2–6V
- Low input current: 1 μ A maximum
- Low quiescent current: 80 μ A maximum
- Compatible with bus-oriented systems
- Output drive capability: 15 LS-TTL loads

Connection Diagram



Top View

Order Number MM54HC534 or MM74HC534

Truth Table

Output Control	Clock	Data	Output
L	↑	H	L
L	↑	L	H
L	L	X	\bar{Q}_0
H	X	X	Z

H = High Level, L = Low Level
 X = Don't Care
 ↑ = Transition from low-to-high
 Z = High impedance state
 \bar{Q}_0 = The level of the output before steady state input conditions were established

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Absolute Maximum Ratings (Notes 1 & 2)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{CC})	-0.5 to +7.0V
DC Input Voltage (V_{IN})	-1.5 to $V_{CC} + 1.5V$
DC Output Voltage (V_{OUT})	-0.5 to $V_{CC} + 0.5V$
Clamp Diode Current (I_{IK}, I_{OK})	± 20 mA
DC Output Current, per pin (I_{OUT})	± 35 mA
DC V_{CC} or GND Current, per pin (I_{CC})	± 70 mA
Storage Temperature Range (T_{STG})	-65°C to +150°C
Power Dissipation (P_D) (Note 3)	600 mW
S.O. Package only	500 mW
Lead Temperature (T_L) (Soldering 10 seconds)	260°C

Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC})	2	6	V
DC Input or Output Voltage (V_{IN}, V_{OUT})	0	V_{CC}	V
Operating Temp. Range (T_A)			
MM74HC	-40	+85	°C
MM54HC	-55	+125	°C
Input Rise or Fall Times (t_r, t_f)			
$V_{CC} = 2.0V$		1000	ns
$V_{CC} = 4.5V$		500	ns
$V_{CC} = 6.0V$		400	ns

DC Electrical Characteristics (Note 4)

Symbol	Parameter	Conditions	V_{CC}	$T_A = 25^\circ C$			Units	
				Typ	74HC $T_A = -40$ to $85^\circ C$	54HC $T_A = -55$ to $125^\circ C$		
V_{IH}	Minimum High Level Input Voltage		2.0V	1.5	1.5	1.5	V	
			4.5V	3.15	3.15	3.15	V	
			6.0V	4.2	4.2	4.2	V	
V_{IL}	Maximum Low Level Input Voltage**		2.0V	0.5	0.5	0.5	V	
			4.5V	1.35	1.35	1.35	V	
			6.0V	1.8	1.8	1.8	V	
V_{OH}	Minimum High Level Output Voltage	$V_{IN} = V_{IH}$ or V_{IL} $ I_{OUT} \leq 20 \mu A$	2.0V	2.0	1.9	1.9	V	
			4.5V	4.5	4.4	4.4	V	
			6.0V	6.0	5.9	5.9	V	
		$V_{IN} = V_{IH}$ or V_{IL} $ I_{OUT} \leq 6.0$ mA $ I_{OUT} \leq 7.8$ mA	4.5V	4.2	3.98	3.84	3.7	V
			6.0V	5.7	5.48	5.34	5.2	V
V_{OL}	Maximum Low Level Output Voltage	$V_{IN} = V_{IH}$ or V_{IL} $ I_{OUT} \leq 20 \mu A$	2.0V	0	0.1	0.1	0.1	V
			4.5V	0	0.1	0.1	0.1	V
			6.0V	0	0.1	0.1	0.1	V
		$V_{IN} = V_{IH}$ or V_{IL} $ I_{OUT} \leq 6.0$ mA $ I_{OUT} \leq 7.8$ mA	4.5V	0.2	0.26	0.33	0.4	V
			6.0V	0.2	0.26	0.33	0.4	V
I_{IN}	Maximum Input Current	$V_{IN} = V_{CC}$ or GND	6.0V		± 0.1	± 1.0	± 1.0	μA
I_{OZ}	Maximum TRI-STATE Output Leakage Current	$V_{IN} = V_{IH}$ or $V_{IL}, OC = V_{IH}$ $V_{OUT} = V_{CC}$ or GND	6.0V		± 0.5	± 5	± 10	μA
I_{CC}	Maximum Quiescent Supply Current	$V_{IN} = V_{CC}$ or GND $I_{OUT} = 0 \mu A$	6.0V		8.0	80	160	μA

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power Dissipation temperature derating — plastic "N" package: -12 mW/°C from 65°C to 85°C; ceramic "J" package: -12 mW/°C from 100°C to 125°C.

Note 4: For a power supply of 5V $\pm 10\%$ the worst case output voltages (V_{OH} , and V_{OL}) occur for HC at 4.5V. Thus the 4.5V values should be used when designing with this supply. Worst case V_{IH} and V_{IL} occur at $V_{CC} = 5.5V$ and 4.5V respectively. (The V_{IH} value at 5.5V is 3.85V.) The worst case leakage current (I_{IN} , I_{CC} , and I_{OZ}) occur for CMOS at the higher voltage and so the 6.0V values should be used.

** V_{IL} limits are currently tested at 20% of V_{CC} . The above V_{IL} specification (30% of V_{CC}) will be implemented no later than Q1, CY'89.

AC Electrical Characteristics $V_{CC}=5V, T_A=25^{\circ}C, t_r=t_f=6\text{ ns}$

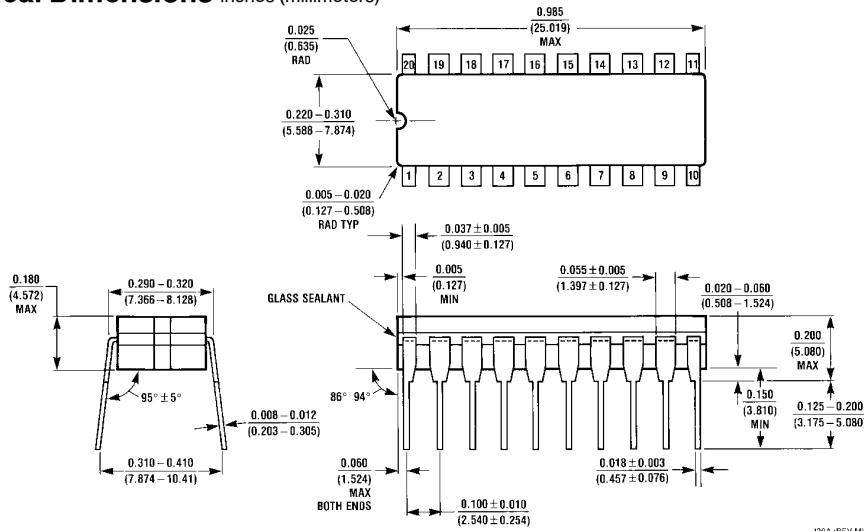
Symbol	Parameter	Conditions	Typ	Guaranteed Limit	Units
f _{MAX}	Maximum Operating Frequency			35	MHz
t _{PHL} , t _{PLH}	Maximum Propagation Delay Clock to \bar{Q}	C _L = 45 pF	23	32	ns
t _{PZH} , t _{PZL}	Maximum Output Enable Time	R _L = 1 kΩ C _L = 45 pF	21	28	ns
t _{PHZ} , t _{PLZ}	Maximum Output Disable Time	R _L = 1 kΩ C _L = 5 pF	19	25	ns
t _S	Minimum Setup Time		10	20	ns
t _H	Minimum Hold Time		0	5	ns
t _W	Minimum Pulse Width		9	16	ns

AC Electrical Characteristics $V_{CC}=2.0-6.0V, C_L=50\text{ pF}, t_r=t_f=6\text{ ns}$ (unless otherwise specified)

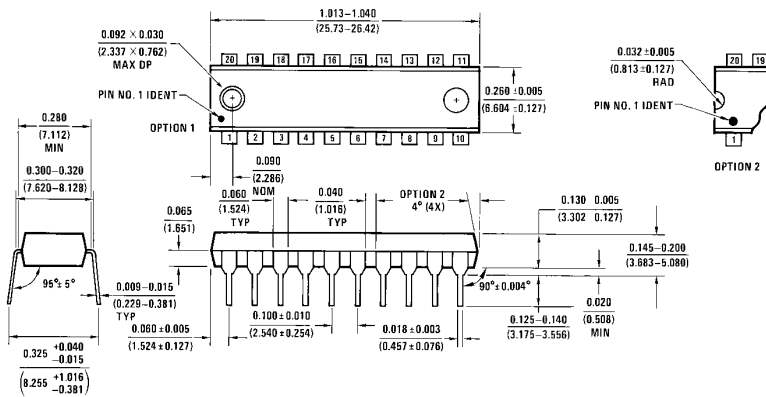
Symbol	Parameter	Conditions	V _{CC}	T _A = 25°C			Units
				Typ	74HC T _A = -40 to 85°C	54HC T _A = -55 to 125°C	
f _{MAX}	Maximum Operating Frequency	C _L = 50 pF	2.0V	6	5	4	MHz
			4.5V	30	24	20	MHz
			6.0V	35	28	23	MHz
t _{PHL} , t _{PLH}	Maximum Propagation Delay, Clock to \bar{Q}	C _L = 50 pF	2.0V	68	180	225	ns
			4.5V	22	36	45	ns
		C _L = 150 pF	2.0V	110	230	288	ns
			4.5V	30	46	57	ns
t _{PZH} , t _{PZL}	Maximum Output Enable Time	R _L = 1 kΩ	2.0V	50	150	189	ns
			4.5V	21	30	37	ns
		C _L = 50 pF	2.0V	80	200	250	ns
			4.5V	29	40	50	ns
t _{PHZ} , t _{PLZ}	Maximum Output Disable Time	R _L = 1 kΩ	2.0V	19	26	31	ns
			4.5V	25	35	44	ns
		C _L = 50 pF	2.0V	50	150	189	ns
			4.5V	21	30	37	ns
t _S	Minimum Setup Time		2.0V	50	60	75	ns
			4.5V	9	13	15	ns
			6.0V	9	11	13	ns
t _H	Minimum Hold Time		2.0V	5	5	5	ns
			4.5V	5	5	5	ns
			6.0V	5	5	5	ns
t _W	Minimum Pulse Width		2.0V	80	100	120	ns
			4.5V	16	20	24	ns
			6.0V	14	18	20	ns
t _{THL} , t _{TLH}	Maximum Output Rise and Fall Time	C _L = 50 pF	2.0V	25	60	75	ns
			4.5V	7	12	15	ns
			6.0V	6	10	13	ns
t _r , t _f	Maximum Input Rise and Fall Time Clock			1000	1000	1000	ns
				500	500	500	ns
				400	400	400	ns
C _{PD}	Power Dissipation Capacitance (Note 5)	(per flip-flop) OC = V _{CC} OC = Gnd	30 50			pF pF	
C _{IN}	Maximum Input Capacitance		5	10	10	pF	
C _{OUT}	Maximum Output Capacitance		15	20	20	pF	

Note 5: C_{PD} determines the no load dynamic power consumption, P_D = C_{PD} V_{CC}² f + I_{CC} V_{CC}, and the no load dynamic current consumption, I_S = C_{PD} V_{CC} f + I_{CC}.

Physical Dimensions inches (millimeters)



Ceramic Dual-In-Line Package (J)
Order Number MM54HC534J or MM74HC534J
NS Package J20A



Molded Dual-In-Line Package (N)
Order Number MM74HC534N
NS Package N20A

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