National Semiconductor

PRELIMINARY

MM54HC4560/MM74HC4560 4 Bit BCD Adder

General Description

This silicon gate CMOS adder performs the addition at LS-TTL speeds of two 4-bit numbers in NBCD (natural binary coded decimal) format, resulting in sum and carry outputs in NBCD code.

This device can also subtract when one set of inputs is 9's Complemented

All inputs and outputs are active high. The carry input for the least significant digit is connected to GND for no carry in.

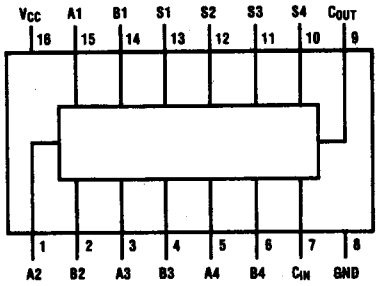
All inputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

Features

- Wide supply range: 2V to 6V
- Low quiescent consumption: 8 μA at 25°C
- Low input current: <1 μA
- Fanout of 10 LS-TTL loads

Connection Diagram

Dual-In-Line Package



TL/F/5374–1

MM54HC4560/MM74HC4560

54HC4560 (J) 74HC4560 (J,N)

Truth Table*

INPUT									OUTPUT				
A4	A3	A2	A1	B4	B3	B2	B1	C_{IN}	C_{OUT}	S4	S3	S2	S1
0	0	0	0	0	0	0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0	1	0	0	0	0	1
0	1	0	0	0	0	1	1	0	0	0	1	1	1
0	1	0	0	0	0	1	1	1	0	1	0	0	0
0	1	1	1	0	1	0	0	0	1	0	0	0	1
0	1	1	1	0	1	0	0	1	1	0	0	1	0
1	0	0	0	0	1	0	1	0	1	0	0	1	1
0	1	1	0	1	0	0	0	0	1	0	1	0	0
1	0	1	1	1	0	0	1	1	1	1	0	0	1

*Partial truth table to show logic operation for representative input values

Absolute Maximum Ratings (Notes 1 and 2)

Supply Voltage (V_{CC})	−0.5 to +7.0V
DC Input Voltage (V_{IN})	−1.5 to V_{CC}+1.5V
DC Output Voltage (V_{OUT})	−0.5 to V_{CC}+0.5V
Clamp Diode Current (I_{IK}, I_{OK})	±20 mA
DC Output Current, per pin (I_{OUT})	±25 mA
DC V_{CC} or GND Current, per pin (I_{CC})	±50 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
Power Dissipation (P_D) (Note 3)	500 mW
Lead Temperature (T_L) (Soldering 10 seconds)	300°C

Operating Conditions

	Min	Max	Units
Supply Voltage(V_{CC})	2	6	V
DC Input or Output Voltage (V_{IN},V_{OUT})	0	V_{CC}	V
Operating Temperature Range(T_A)			
MM74HC	−40	+85	°C
MM54HC	−55	+125	°C
Input Rise or Fall Times (t_r, t_f) V_{CC}=2.0V		1000	ns
V_{CC}=4.5V		500	ns
V_{CC}=6.0V		400	ns

DC Electrical Characteristics (Note 4)

Symbol	Parameter	Conditions	V_{CC}	T_A=25°C	74HC T_A=−40 to 85°C	54HC T_A=−55 to 125°C	Units
				Typ	Guaranteed Limits		
V_{IH}	Minimum High Level Input Voltage		2.0V		1.5	1.5	1.5	V
			4.5V		3.15	3.15	3.15	V
			6.0V		4.2	4.2	4.2	V
V_{IL}	Maximum Low Level Input Voltage		2.0V		0.3	0.3	0.3	V
			4.5V		0.9	0.9	0.9	V
			6.0V		1.2	1.2	1.2	V
V_{OH}	Minimum High Level Output Voltage	V_{IN}=V_{IH} or V_{IL} |I_{OUT}|≤20 μA	2.0V	2.0	1.9	1.9	1.9	V
			4.5V	4.5	4.4	4.4	4.4	V
			6.0V	6.0	5.9	5.9	5.9	V
		V_{IN}=V_{IH} or V_{IL} |I_{OUT}|≤4.0 mA	4.5V	4.2	3.98	3.84	3.7	V
		|I_{OUT}|≤5.2 mA	6.0V	5.7	5.48	5.34	5.2	V
V_{OL}	Maximum Low Level Output Voltage	V_{IN}=V_{IH} or V_{IL} |I_{OUT}|≤20 μA	2.0V	0	0.1	0.1	0.1	V
			4.5V	0	0.1	0.1	0.1	V
			6.0V	0	0.1	0.1	0.1	V
		V_{IN}=V_{IH} or V_{IL} |I_{OUT}|≤4 mA	4.5V	0.2	0.26	0.33	0.4	V
		|I_{OUT}|≤5.2 mA	6.0V	0.2	0.26	0.33	0.4	V
I_{IN}	Maximum Input Current	V_{IN}=V_{CC} or GND	6.0V		±0.1	±1.0	±1.0	μA
I_{CC}	Maximum Quiescent Supply Current	V_{IN}=V_{CC} or GND I_{OUT}=0 μA	6.0V		8	80	160	μA

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power Dissipation temperature derating — plastic "N" package: −12 mW/°C from 65°C to 85°C; ceramic "J" package: −12 mW/°C from 100°C to 125°C.

Note 4: For a power supply of 5V ±10% the worst case output voltages (V_{OH}, and V_{OL}) occur for HC at 4.5V. Thus the 4.5V values should be used when designing with this supply. Worst case V_{IH} and V_{IL} occur at V_{CC}=5.5V and 4.5V respectively. (The V_{IH} value at 5.5V is 3.85V.) The worst case leakage current (I_{IN}, I_{CC}, and I_{OZ}) occur for CMOS at the higher voltage and so the 6.0V values should be used.

AC Electrical Characteristics

$V_{CC}=5V$, $T_A=25°C$, $C_L=15$ pF, $t_r=t_f=6$ ns

Symbol	Parameter	Conditions	Typ	Guaranteed Limit	Units
t_{PHL}, t_{PLH}	Maximum Propagation Delay From A or B to Sn			30	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay From A or B to C_{OUT}			30	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay From C_{IN} to C_{OUT}			25	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay From C_{IN} to Sn			25	ns

AC Electrical Characteristics

$C_L=50$ pF, $t_r=t_f=6$ ns (unless otherwise specified)

Symbol	Parameter	Conditions	V_{CC}	$T_A=25°C$	74HC $T_A=-40$ to 85°C	54HC $T_A=-55$ to 125°C	Units
				Typ	Guaranteed Limits		
t_{PHL}, t_{PLH}	Maximum Propagation Delay From A or B to Sn		2.0V	75	175	219	262	ns
			4.5V	21	35	44	53	ns
			6.0V	18	30	38	45	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay From A or B to C_{OUT}		2.0V	73	175	219	262	ns
			4.5V	20	35	44	53	ns
			6.0V	18	30	38	45	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay From C_{IN} to C_{OUT}		2.0V	63	150	189	225	ns
			4.5V	18	30	38	45	ns
			6.0V	16	26	32	39	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay From C_{IN} to Sn		2.0V	63	150	189	225	ns
			4.5V	18	30	38	45	ns
			6.0V	16	26	32	39	ns
t_{THL}, t_{TLH}	Maximum Output Rise and Fall Time		2.0V	30	75	95	110	ns
			4.5V	8	15	19	22	ns
			6.0V	6	13	16	19	ns
C_{IN}	Maximum Input Capacitance			5	10	10	10	μF
C_{PD}	Power Dissipation Capacitance	(Note 5)						μF

Note 5: C_{PD} determines the no load dynamic power consumption, $P_D=C_{PD}\ V_{CC}^2\ f+I_{CC}\ V_{CC}$, and the no load dynamic current consumption, $I_S=C_{PD}\ V_{CC}\ f+I_{CC}$.

Note 6: Refer to Section 1 for Typical MM54/74HC AC Switching Waveforms and Test Circuits.