

74HC4520; 74HCT4520

Dual 4-bit synchronous binary counter

Rev. 4 — 10 May 2016

Product data sheet

1. General description

The 74HC4520; 74HCT4520 are dual 4-bit internally synchronous binary counters with two clock inputs ($nCP0$ and $n\overline{CP1}$). They have buffered outputs from all 4 bit positions ($nQ0$ to $nQ3$) and an asynchronous master reset input (nMR). The counter advances on the LOW-to-HIGH transition of $nCP0$ when $n\overline{CP1}$ is HIGH. It also advances on the HIGH-to-LOW transition of $n\overline{CP1}$ when $nCP0$ is LOW. Either $nCP0$ or $n\overline{CP1}$ may be used as the clock input to the counter. The other clock input may be used as a clock enable input. A HIGH on nMR , resets the counter ($nQ0$ to $nQ3 = \text{LOW}$) independent of $nCP0$ and $n\overline{CP1}$. Inputs include clamp diodes. It enables the use of current limiting resistors to interface inputs to voltages in excess of V_{CC} .

2. Features and benefits

- Complies with JEDEC standard no. 7A
- Input levels:
 - ◆ For 74HC4520: CMOS level
 - ◆ For 74HCT4520: TTL level
- ESD protection:
 - ◆ HBM JESD22-A114F exceeds 2000 V
 - ◆ MM JESD22-A115-A exceeds 200 V
- Multiple package options
- Specified from $-40\text{ }^{\circ}\text{C}$ to $+85\text{ }^{\circ}\text{C}$ and $-40\text{ }^{\circ}\text{C}$ to $+125\text{ }^{\circ}\text{C}$

3. Applications

- Multistage synchronous counting
- Multistage asynchronous counting
- Frequency dividers

4. Ordering information

Table 1. Ordering information

Type number	Package			Version
	Temperature range	Name	Description	
74HC4520D 74HCT4520D	-40 °C to +125 °C	SO16	plastic small outline package; 16 leads; body width 3.9 mm	SOT109-1
74HC4520DB 74HCT4520DB	-40 °C to +125 °C	SSOP16	plastic shrink small outline package; 16 leads; body width 5.3 mm	SOT338-1
74HC4520PW	-40 °C to +125 °C	TSSOP16	plastic thin shrink small outline package; 16 leads; body width 4.4 mm	SOT403-1

5. Functional diagram

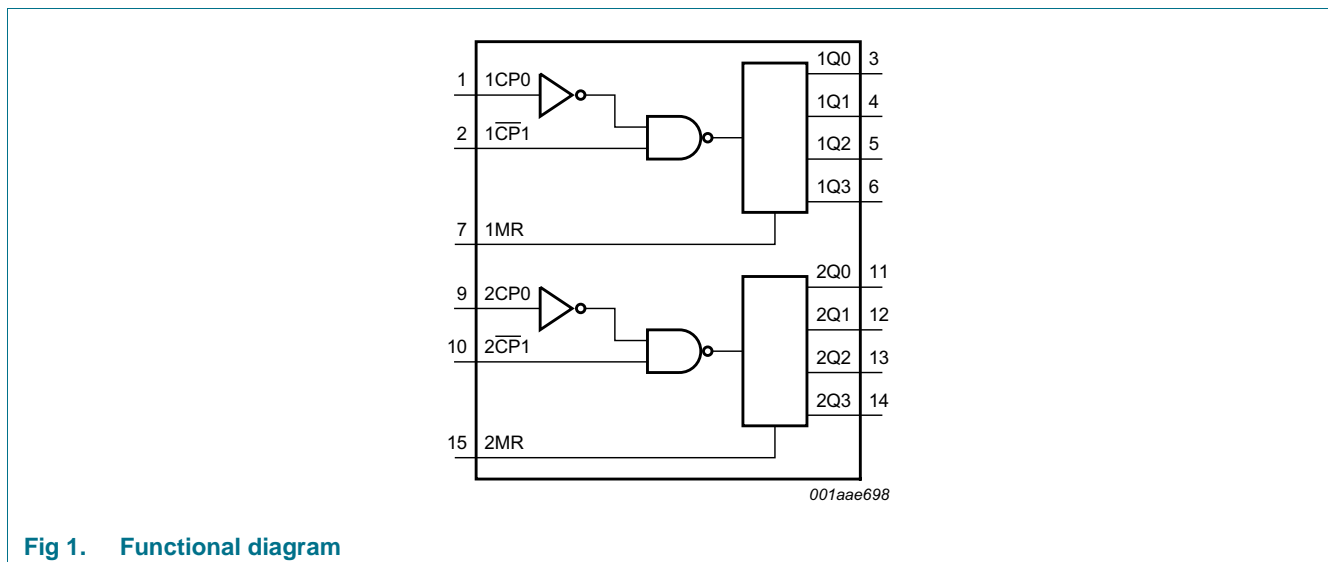


Fig 1. Functional diagram

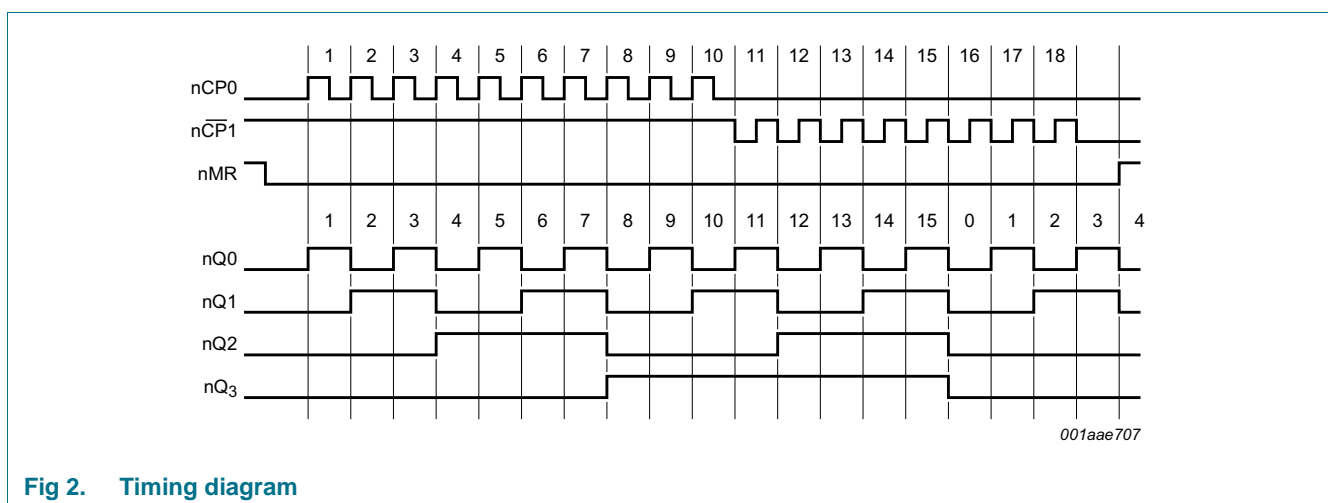


Fig 2. Timing diagram

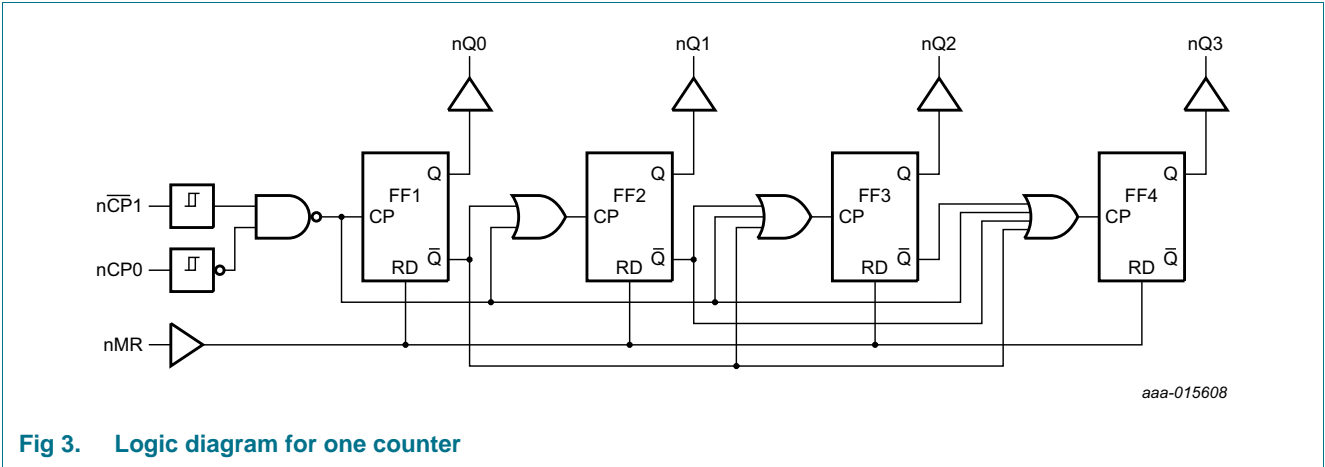


Fig 3. Logic diagram for one counter

6. Pinning information

6.1 Pinning

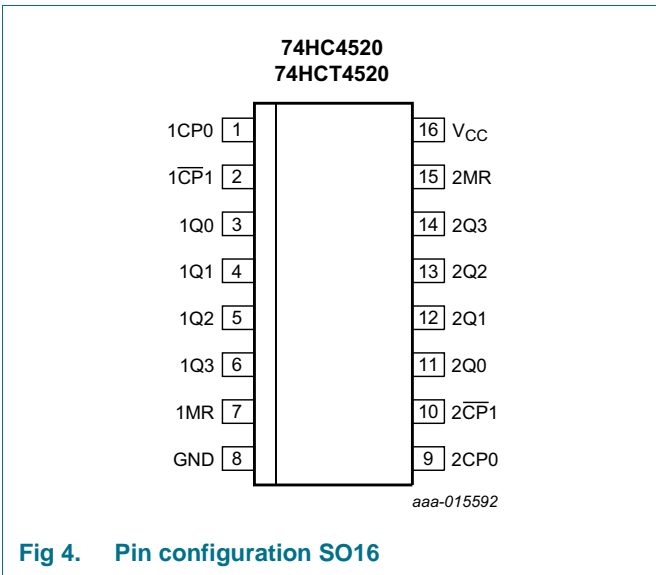


Fig 4. Pin configuration SO16

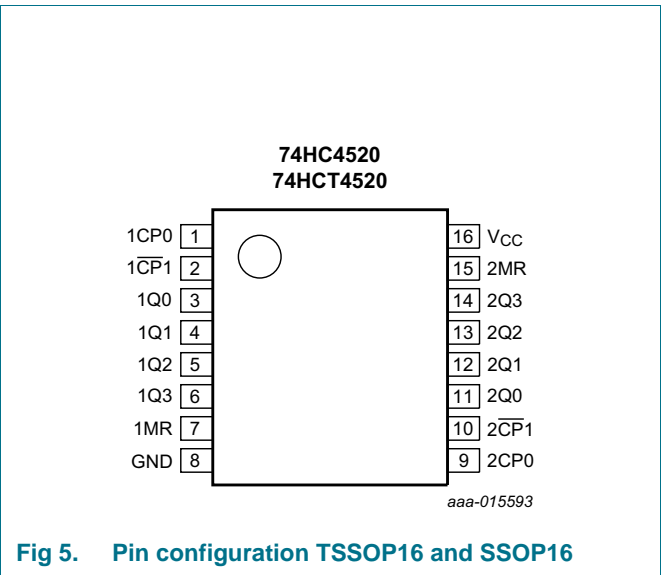


Fig 5. Pin configuration TSSOP16 and SSOP16

6.2 Pin description

Table 2. Pin description

Symbol	Pin	Description
1CP0, 2CP0	1, 9	clock input (LOW-to-HIGH edge-triggered)
1CP1, 2CP1	2, 10	clock input (HIGH-to-LOW edge-triggered)
1Q0 to 1Q3	3, 4, 5, 6	output
1MR, 2MR	7, 15	asynchronous master reset input (active HIGH)
GND	8	ground (0 V)
2Q0 to 2Q3	11, 12, 13, 14	output
V _{CC}	16	supply voltage

7. Functional description

Table 3. Function table^[1]

nCP0	nCP1	nMR	Mode
↑	H	L	counter advances
L	↓	L	counter advances
↓	X	L	no change
X	↑	L	no change
↑	L	L	no change
H	↓	L	no change
X	X	H	nQ0 to nQ3 = LOW

[1] H = HIGH voltage level; L = LOW voltage level; X = don't care; ↑ = positive-going transition; ↓ = negative-going transition.

8. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	supply voltage		-0.5	+7.0	V
I_{IK}	input clamping current	$V_I < -0.5\text{ V}$ or $V_I > V_{CC} + 0.5\text{ V}$	-	±20	mA
I_{OK}	output clamping current	$V_O < -0.5\text{ V}$ or $V_O > V_{CC} + 0.5\text{ V}$	-	±20	mA
I_O	output current	$V_O = -0.5\text{ V}$ to $V_{CC} + 0.5\text{ V}$	-	±25	mA
I_{CC}	supply current		-	50	mA
I_{GND}	ground current		-50	-	mA
T_{stg}	storage temperature		-65	+150	°C
P_{tot}	total power dissipation	SO16 and (T)SSOP16 package ^[1]	-	500	mW

[1] For SO16 package: above 70 °C the value of P_{tot} derates linearly at 8 mW/K.
For (T)SSOP16 packages: above 60 °C the value of P_{tot} derates linearly at 5.5 mW/K.

9. Recommended operating conditions

Table 5. Recommended operating conditions

Voltages are referenced to GND (ground = 0 V)

Symbol	Parameter	Conditions	74HC4520			74HCT4520			Unit
			Min	Typ	Max	Min	Typ	Max	
V _{CC}	supply voltage		2.0	5.0	6.0	4.5	5.0	5.5	V
V _I	input voltage		0	-	V _{CC}	0	-	V _{CC}	V
V _O	output voltage		0	-	V _{CC}	0	-	V _{CC}	V
T _{amb}	ambient temperature		-40	+25	+125	-40	+25	+125	°C
Δt/ΔV	input transition rise and fall rate	V _{CC} = 2.0 V	-	-	625	-	-	-	ns/V
		V _{CC} = 4.5 V	-	1.67	139	-	1.67	139	ns/V
		V _{CC} = 6.0 V	-	-	83	-	-	-	ns/V

10. Static characteristics

Table 6. Static characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
74HC4520										
V _{IH}	HIGH-level input voltage	V _{CC} = 2.0 V	1.5	1.2	-	1.5	-	1.5	-	V
		V _{CC} = 4.5 V	3.15	2.4	-	3.15	-	3.15	-	V
		V _{CC} = 6.0 V	4.2	3.2	-	4.2	-	4.2	-	V
V _{IL}	LOW-level input voltage	V _{CC} = 2.0 V	-	0.8	0.5	-	0.5	-	0.5	V
		V _{CC} = 4.5 V	-	2.1	1.35	-	1.35	-	1.35	V
		V _{CC} = 6.0 V	-	2.8	1.8	-	1.8	-	1.8	V
V _{OH}	HIGH-level output voltage	V _I = V _{IH} or V _{IL}								
		I _O = -20 μA; V _{CC} = 2.0 V	1.9	2.0	-	1.9	-	1.9	-	V
		I _O = -20 μA; V _{CC} = 4.5 V	4.4	4.5	-	4.4	-	4.4	-	V
		I _O = -20 μA; V _{CC} = 6.0 V	5.9	6.0	-	5.9	-	5.9	-	V
		I _O = -4.0; V _{CC} = 4.5 V	3.98	4.32	-	3.84	-	3.7	-	V
I _O = -5.2; V _{CC} = 6.0 V	5.48	5.81	-	5.34	-	5.2	-	V		
V _{OL}	LOW-level output voltage	V _I = V _{IH} or V _{IL}								
		I _O = 20 μA; V _{CC} = 2.0 V	-	0	0.1	-	0.1	-	0.1	V
		I _O = 20 μA; V _{CC} = 4.5 V	-	0	0.1	-	0.1	-	0.1	V
		I _O = 20 μA; V _{CC} = 6.0 V	-	0	0.1	-	0.1	-	0.1	V
		I _O = 4.0 mA; V _{CC} = 4.5 V	-	0.15	0.26	-	0.33	-	0.4	V
I _O = 5.2 mA; V _{CC} = 6.0 V	-	0.16	0.26	-	0.33	-	0.4	V		
I _I	input leakage current	V _I = V _{CC} or GND; V _{CC} = 6.0 V	-	-	±0.1	-	±1.0	-	±1.0	μA
I _{CC}	supply current	V _I = V _{CC} or GND; I _O = 0 A; V _{CC} = 6.0 V	-	-	8.0	-	80.0	-	160.0	μA

Table 6. Static characteristics ...continued

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
C _I	input capacitance		-	3.5	-	-	-	-	-	pF
74HCT4520										
V _{IH}	HIGH-level input voltage	V _{CC} = 4.5 V to 5.5 V	2.0	1.6	-	2.0	-	2.0	-	V
V _{IL}	LOW-level input voltage	V _{CC} = 4.5 V to 5.5 V	-	1.2	0.8	-	0.8	-	0.8	V
V _{OH}	HIGH-level output voltage	V _I = V _{IH} or V _{IL} ; V _{CC} = 4.5 V								
		I _O = -20 µA	4.4	4.5	-	4.4	-	4.4	-	V
		I _O = -4.0 mA	3.98	4.32	-	3.84	-	3.7	-	V
V _{OL}	LOW-level output voltage	V _I = V _{IH} or V _{IL} ; V _{CC} = 4.5 V								
		I _O = 20 µA	-	0	0.1	-	0.1	-	0.1	V
		I _O = 4.0 mA	-	0.15	0.26	-	0.33	-	0.4	V
I _I	input leakage current	V _I = V _{CC} or GND; V _{CC} = 5.5 V	-	-	±0.1	-	±1.0	-	±1.0	µA
I _{CC}	supply current	V _I = V _{CC} or GND; I _O = 0 A; V _{CC} = 5.5 V	-	-	8.0	-	80.0	-	160.0	µA
ΔI _{CC}	additional supply current	per input pin; V _I = V _{CC} - 2.1 V; other inputs at V _{CC} or GND; V _{CC} = 4.5 V to 5.5 V; I _O = 0 A								
		pin nCP0, nCP1	-	80	288	-	360	-	392	µA
		pin nMR	-	150	540	-	675	-	735	µA
C _I	input capacitance		-	3.5	-	-	-	-	-	pF

11. Dynamic characteristics

Table 7. Dynamic characteristicsVoltages are referenced to GND (ground = 0 V); C_L = 50 pF unless otherwise specified; for test circuit, see [Figure 7](#).

Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
74HC4520										
t _{pd}	propagation delay	nCP0 to nQn; see Figure 6 ^[1]								
		V _{CC} = 2.0 V	-	77	240	-	300	-	360	ns
		V _{CC} = 4.5 V	-	28	48	-	60	-	72	ns
		V _{CC} = 5.0 V; C _L = 15 pF	-	24	-	-	-	-	-	ns
		V _{CC} = 6.0 V	-	22	41	-	51	-	61	ns
		nCP1 to nQn; see Figure 6 ^[1]								
		V _{CC} = 2.0 V	-	77	240	-	300	-	360	ns
		V _{CC} = 4.5 V	-	28	48	-	60	-	72	ns
		V _{CC} = 5.0 V; C _L = 15 pF	-	24	-	-	-	-	-	ns
V _{CC} = 6.0 V	-	22	41	-	51	-	61	ns		

Table 7. Dynamic characteristics ...continued

Voltages are referenced to GND (ground = 0 V); $C_L = 50$ pF unless otherwise specified; for test circuit, see [Figure 7](#).

Symbol	Parameter	Conditions	25 °C			–40 °C to +85 °C		–40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
t _{PHL}	HIGH to LOW propagation delay	nMR to nQn; see Figure 6								
		V _{CC} = 2.0 V	-	44	150	-	190	-	225	ns
		V _{CC} = 4.5 V	-	16	30	-	38	-	45	ns
		V _{CC} = 5.0 V; C _L = 15 pF	-	13	-	-	-	-	-	ns
		V _{CC} = 6.0 V	-	13	26	-	33	-	38	ns
t _t	transition time	nQn; see Figure 6 ^[2]								
		V _{CC} = 2.0 V	-	19	75	-	95	-	110	ns
		V _{CC} = 4.5 V	-	7	15	-	19	-	22	ns
		V _{CC} = 6.0 V	-	6	13	-	16	-	19	ns
t _w	pulse width	nCP0, nCP1 HIGH or LOW; see Figure 6								
		V _{CC} = 2.0 V	80	22	-	100	-	120	-	ns
		V _{CC} = 4.5 V	16	8	-	20	-	24	-	ns
		V _{CC} = 6.0 V	14	6	-	17	-	20	-	ns
		nMR HIGH; see Figure 6								
		V _{CC} = 2.0 V	120	39	-	150	-	180	-	ns
		V _{CC} = 4.5 V	24	14	-	30	-	36	-	ns
		V _{CC} = 6.0 V	20	11	-	26	-	31	-	ns
t _{rec}	recovery time	nMR to nCP0, nCP1; see Figure 6								
		V _{CC} = 2.0 V	0	-28	-	0	-	0	-	ns
		V _{CC} = 4.5 V	0	-10	-	0	-	0	-	ns
		V _{CC} = 6.0 V	0	-8	-	0	-	0	-	ns
t _{su}	set-up time	nCP0 to nCP1; nCP1 to nCP0; see Figure 6								
		V _{CC} = 2.0 V	80	14	-	100	-	120	-	ns
		V _{CC} = 4.5 V	16	5	-	20	-	24	-	ns
		V _{CC} = 6.0 V	14	4	-	17	-	20	-	ns
f _{max}	maximum frequency	nCP0, nCP1; see Figure 6								
		V _{CC} = 2.0 V	6	19	-	4.8	-	4	-	MHz
		V _{CC} = 4.5 V	30	58	-	24	-	20	-	MHz
		V _{CC} = 5.0 V; C _L = 15 pF	-	68	-	-	-	-	-	MHz
		V _{CC} = 6.0 V	35	69	-	28	-	24	-	MHz
C _{PD}	power dissipation capacitance	V _I = GND to V _{CC} ; V _{CC} = 5 V; ^[3] f _i = 1 MHz	-	29	-	-	-	-	-	pF

Table 7. Dynamic characteristics ...continued

Voltages are referenced to GND (ground = 0 V); $C_L = 50$ pF unless otherwise specified; for test circuit, see [Figure 7](#).

Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
74HCT4520										
t_{pd}	propagation delay	nCP0 to nQn; see Figure 6 ^[1]								
		$V_{CC} = 4.5$ V	-	28	53	-	66	-	80	ns
		$V_{CC} = 5.0$ V; $C_L = 15$ pF	-	24	-	-	-	-	-	ns
		n $\overline{CP1}$ to nQn; see Figure 6 ^[1]								
		$V_{CC} = 4.5$ V	-	25	53	-	66	-	80	ns
		$V_{CC} = 5.0$ V; $C_L = 15$ pF	-	24	-	-	-	-	ns	
t_{PHL}	HIGH to LOW propagation delay	nMR to nQn; see Figure 6								
		$V_{CC} = 4.5$ V	-	16	35	-	44	-	53	ns
		$V_{CC} = 5.0$ V; $C_L = 15$ pF	-	13	-	-	-	-	-	ns
t_t	transition time	nQn; see Figure 6 ^[2]								
		$V_{CC} = 4.5$ V	-	7	15	-	19	-	22	ns
t_W	pulse width	nCP0, n $\overline{CP1}$ HIGH or LOW; see Figure 6								
		$V_{CC} = 4.5$ V	20	10	-	25	-	30	-	ns
		nMR HIGH; see Figure 6								
		$V_{CC} = 4.5$ V	20	12	-	25	-	30	-	ns
t_{rec}	recovery time	nMR to nCP0, n $\overline{CP1}$; see Figure 6								
		$V_{CC} = 4.5$ V	0	-8	-	0	-	0	-	ns
t_{su}	set-up time	nCP0 to n $\overline{CP1}$; n $\overline{CP1}$ to nCP0; see Figure 6								
		$V_{CC} = 4.5$ V	16	6	-	20	-	24	-	ns
f_{max}	maximum frequency	nCP0, n $\overline{CP1}$; see Figure 6								
		$V_{CC} = 4.5$ V	30	58	-	24	-	20	-	MHz
		$V_{CC} = 5.0$ V; $C_L = 15$ pF	-	64	-	-	-	-	-	MHz
C_{PD}	power dissipation capacitance	$V_I = \text{GND to } V_{CC} - 1.5$ V; $V_{CC} = 5$ V; $f_i = 1$ MHz ^[3]	-	24	-	-	-	-	-	pF

[1] t_{pd} is the same as t_{PHL} and t_{PLH} .

[2] t_t is the same as t_{THL} and t_{TLH} .

[3] C_{PD} is used to determine the dynamic power dissipation (P_D in μW):

$$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \sum(C_L \times V_{CC}^2 \times f_o) \text{ where:}$$

f_i = input frequency in MHz;

f_o = output frequency in MHz;

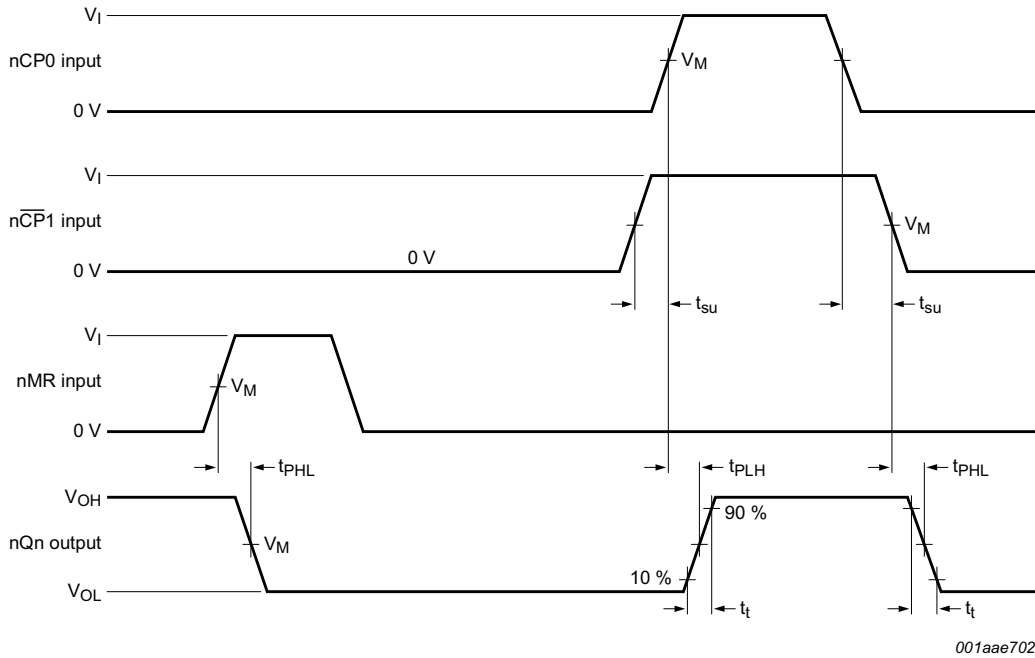
C_L = output load capacitance in pF;

V_{CC} = supply voltage in V;

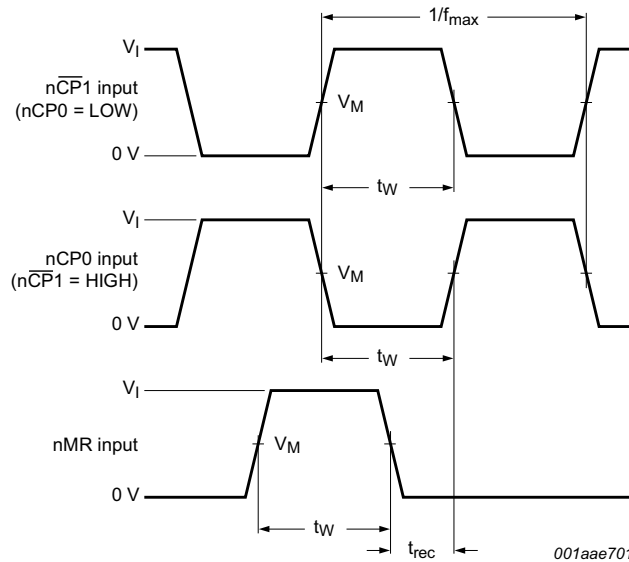
N = number of inputs switching;

$\sum(C_L \times V_{CC}^2 \times f_o)$ = sum of outputs.

12. Waveforms



a. nCP0 and nCP1 set-up times, propagation delays and output transition times



b. nMR recovery time, minimum nCP0, nCP1, nMR pulse widths and maximum frequency

Measurement points are given in [Table 8](#).

The logic levels V_{OH} and V_{OL} are typical output voltage levels that occur with the output load.

Fig 6. Waveforms showing measurements for switching times

Table 8. Measurement points

Type	Input		Output
	V_M	V_I	V_M
74HC4520	$0.5 \times V_{CC}$	GND to V_{CC}	$0.5 \times V_{CC}$
74HCT4520	1.3 V	GND to 3 V	1.3 V

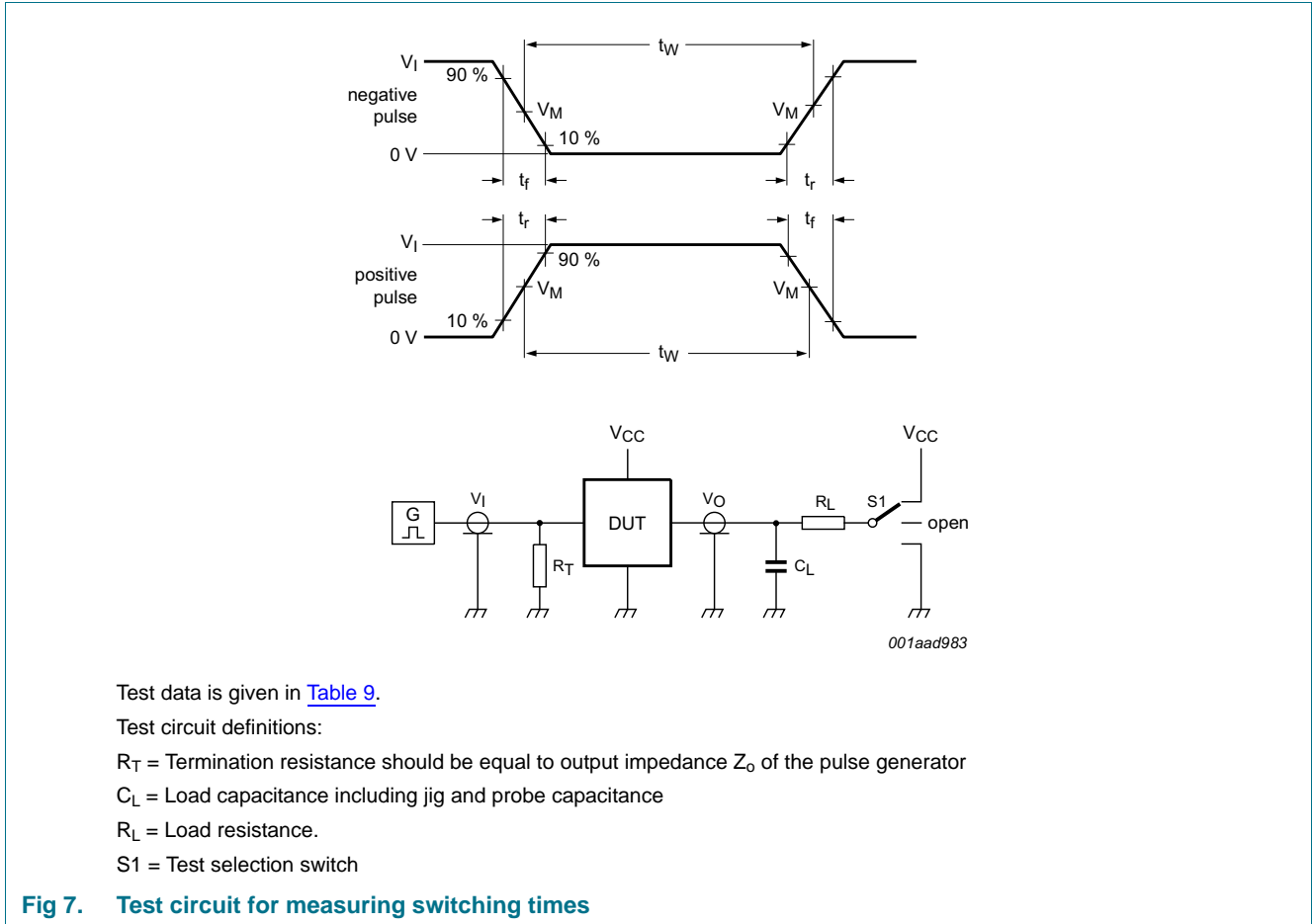


Table 9. Test data

Type	Input		Load		S1 position
	V_I	t_r, t_f	C_L	R_L	t_{PHL}, t_{PLH}
74HC4520	GND to V_{CC}	6 ns	15 pF, 50 pF	1 k Ω	open
74HCT4520	GND to 3 V	6 ns	15 pF, 50 pF	1 k Ω	open

13. Package outline

SO16: plastic small outline package; 16 leads; body width 3.9 mm

SOT109-1

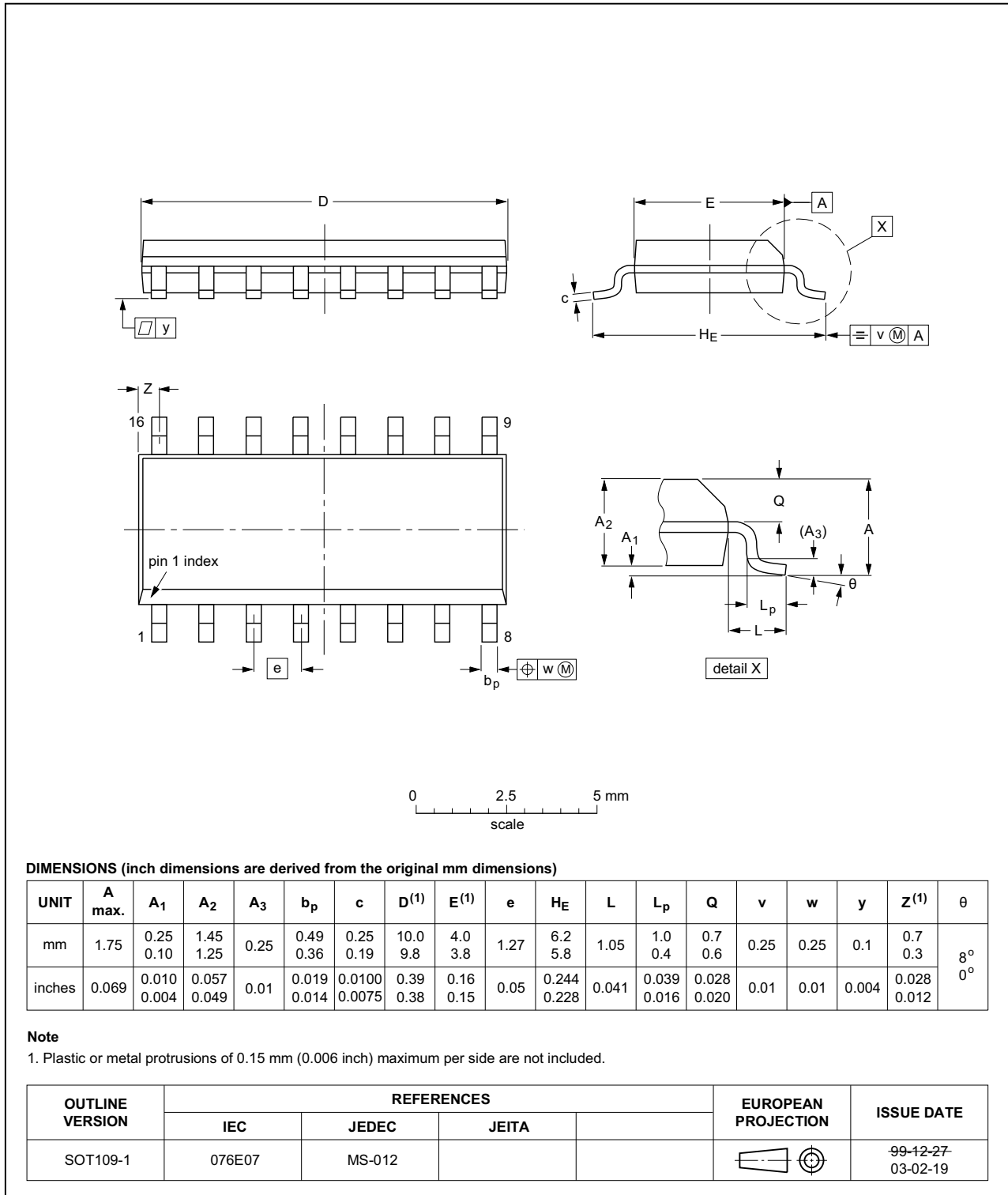


Fig 8. Package outline SOT109-1 (SO16)

SSOP16: plastic shrink small outline package; 16 leads; body width 5.3 mm

SOT338-1

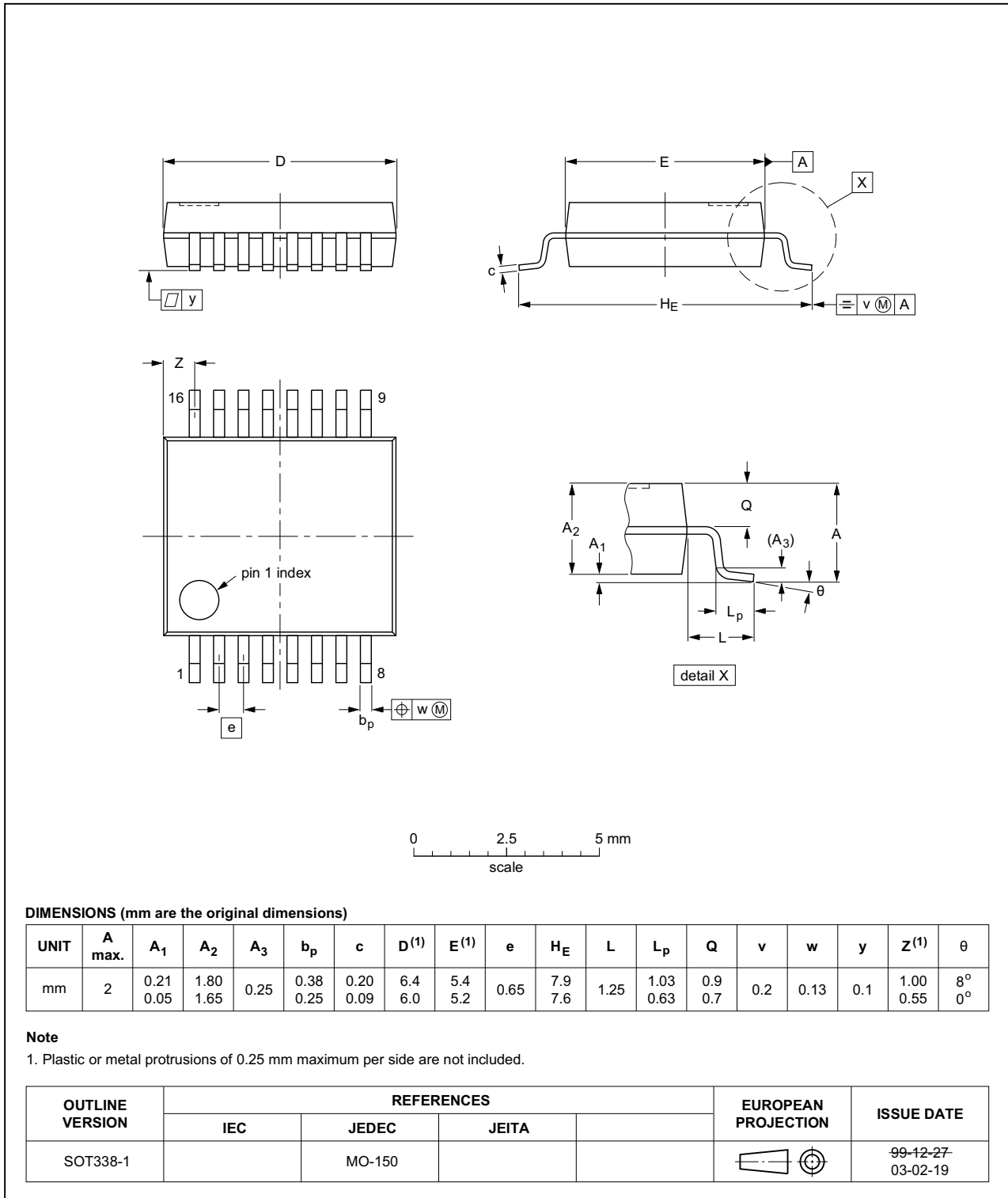


Fig 9. Package outline SOT338-1 (SSOP16)

TSSOP16: plastic thin shrink small outline package; 16 leads; body width 4.4 mm

SOT403-1

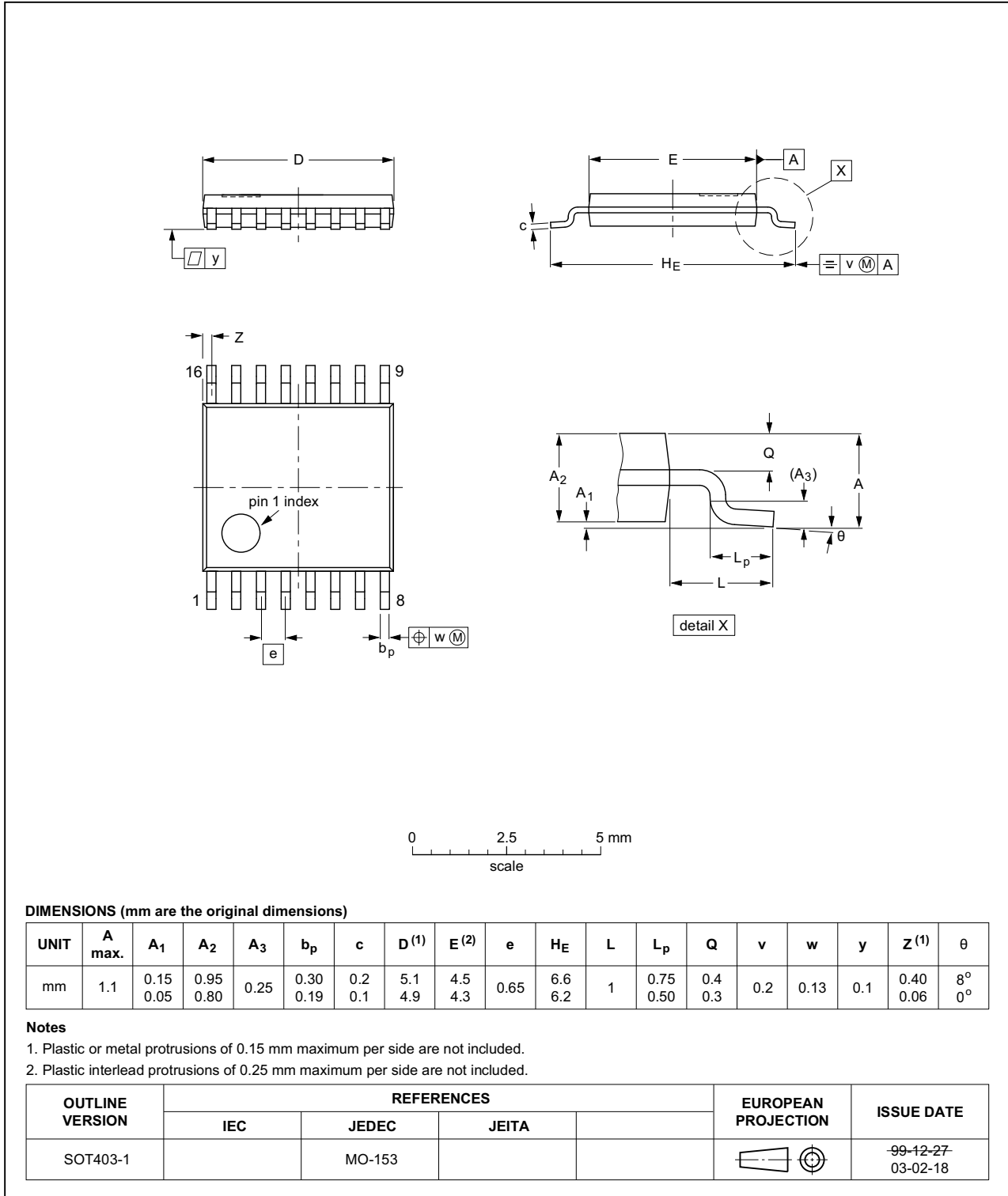


Fig 10. Package outline SOT403-1 (TSSOP16)

14. Abbreviations

Table 10. Abbreviations

Acronym	Description
CMOS	Complementary Metal-Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model
LSTTL	Low-power Schottky Transistor-Transistor Logic
MM	Machine Model
TTL	Transistor-Transistor Logic

15. Revision history

Table 11. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74HC_HCT4520 v.4	20160510	Product data sheet	-	74HC_HCT4520 v.3
Modifications:	<ul style="list-style-type: none"> Type numbers 74HC4520N and 74HCT4520N (SOT38-4) removed. 			
74HC_HCT4520 v.3	20141204	Product data sheet	-	74HC_HCT4520_CNV v.2
Modifications:	<ul style="list-style-type: none"> The format of this data sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors. Legal texts have been adapted to the new company name where appropriate. 			
74HC_HCT4520_CNV v.2	19930927	Product specification	-	-

16. Legal information

16.1 Data sheet status

Document status ^{[1][2]}	Product status ^[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL <http://www.nexperia.com>.

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For more information, please visit: <http://www.nexperia.com>

For sales office addresses, please send an email to: salesaddresses@nexperia.com

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