

# DATA SHEET

For a complete data sheet, please also download:

- The IC06 74HC/HCT/HCU/HCMOS Logic Family Specifications
- The IC06 74HC/HCT/HCU/HCMOS Logic Package Information
- The IC06 74HC/HCT/HCU/HCMOS Logic Package Outlines

## **74HC/HCT40104**

**4-bit bidirectional universal shift register; 3-state**

Product specification  
File under Integrated Circuits, IC06

December 1990

## 4-bit bidirectional universal shift register; 3-state

## 74HC/HCT40104

### FEATURES

- Synchronous parallel or serial operating
- 3-state outputs
- Output capability: bus driver
- I<sub>CC</sub> category: MSI

### GENERAL DESCRIPTION

The 74HC/HCT40104 are high-speed Si-gate CMOS devices and are pin compatible with the "40104" of the "4000B" series. They are specified in compliance with JEDEC standard no. 7A.

The 74HC/HCT40104 are universal shift registers featuring parallel inputs, parallel outputs, shift-right and shift-left serial inputs and 3-state outputs allowing the devices to be used in bus-organized systems.

### QUICK REFERENCE DATA

GND = 0 V; T<sub>amb</sub> = 25 °C; t<sub>r</sub> = t<sub>f</sub> = 6 ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay CP to Q <sub>n</sub>	C <sub>L</sub> = 15 pF; V <sub>CC</sub> = 5 V	13	15	ns
f <sub>max</sub>	maximum clock frequency		62	57	MHz
C <sub>I</sub>	input capacitance		3.5	3.5	pF
C <sub>PD</sub>	power dissipation capacitance per package	notes 1 and 2	75	75	pF

### Notes

1. C<sub>PD</sub> is used to determine the dynamic power dissipation (P<sub>D</sub> in μW):

$$P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum (C_L \times V_{CC}^2 \times f_o) \text{ where:}$$

f<sub>i</sub> = input frequency in MHz

f<sub>o</sub> = output frequency in MHz

∑ (C<sub>L</sub> × V<sub>CC</sub><sup>2</sup> × f<sub>o</sub>) = sum of outputs

C<sub>L</sub> = output load capacitance in pF

V<sub>CC</sub> = supply voltage in V

2. For HC the condition is V<sub>I</sub> = GND to V<sub>CC</sub>  
For HCT the condition is V<sub>I</sub> = GND to V<sub>CC</sub> – 1.5 V

### ORDERING INFORMATION

See "74HC/HCT/HCU/HCMOS Logic Package Information".

In the parallel-load mode (S<sub>0</sub> and S<sub>1</sub> are HIGH), data is loaded into the associated flip-flop and appears at the output after the positive transition of the clock input (CP).

During loading, serial data flow is inhibited. Shift-right and shift-left are accomplished synchronously on the positive clock edge with serial data entered at the shift-right (D<sub>SR</sub>) and shift-left (D<sub>SL</sub>) serial inputs, respectively.

Clearing the register is accomplished by setting both mode controls (S<sub>0</sub> and S<sub>1</sub>) LOW and clocking the register. When the output enable input (OE) is LOW, all outputs assume the high-impedance OFF-state (Z).

### APPLICATIONS

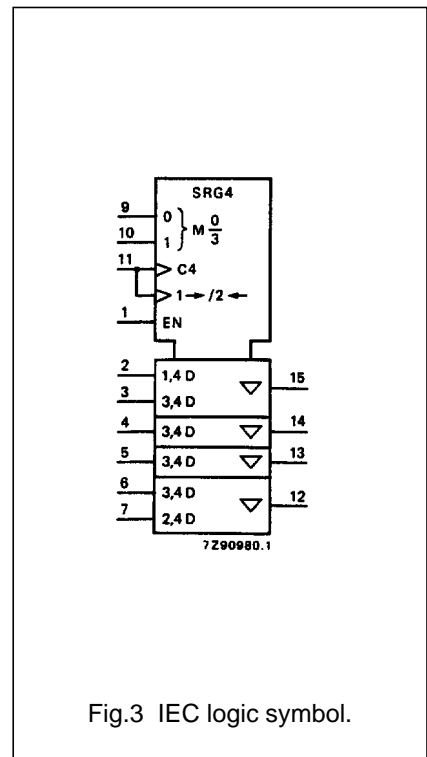
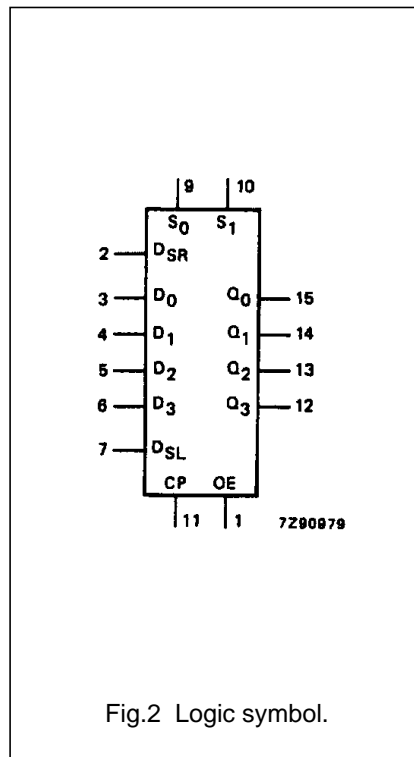
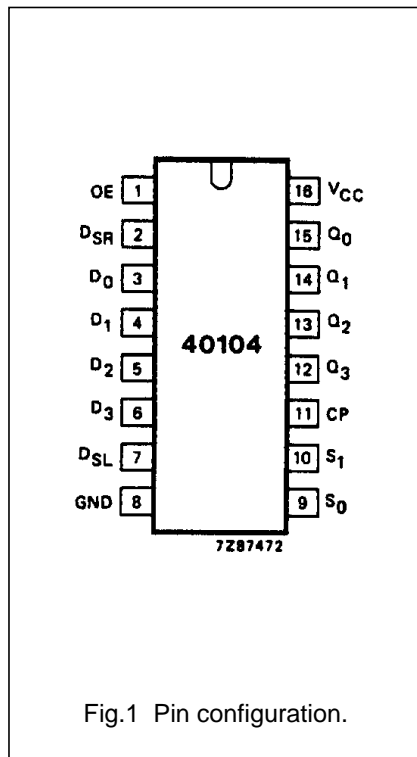
- Arithmetic unit bus registers
- Serial/parallel conversion
- General-purpose register for bus organized systems
- General-purpose registers

4-bit bidirectional universal shift register;  
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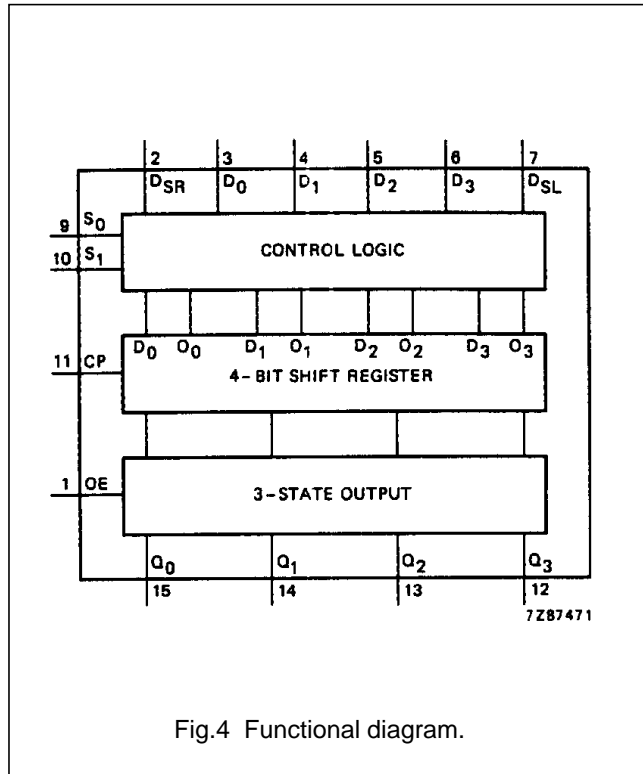
PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
1	OE	3-state output enable input (active HIGH)
2	D <sub>SR</sub>	serial data shift-right input
3, 4, 5, 6	D <sub>0</sub> to D <sub>3</sub>	parallel data inputs
7	D <sub>SL</sub>	serial data shift-left input
8	GND	ground (0 V)
9, 10	S <sub>0</sub> , S <sub>1</sub>	mode control inputs
11	CP	clock input (LOW-to-HIGH, edge-triggered)
15, 14, 13, 12	Q <sub>0</sub> to Q <sub>3</sub>	3-state parallel outputs
16	V <sub>CC</sub>	positive supply voltage



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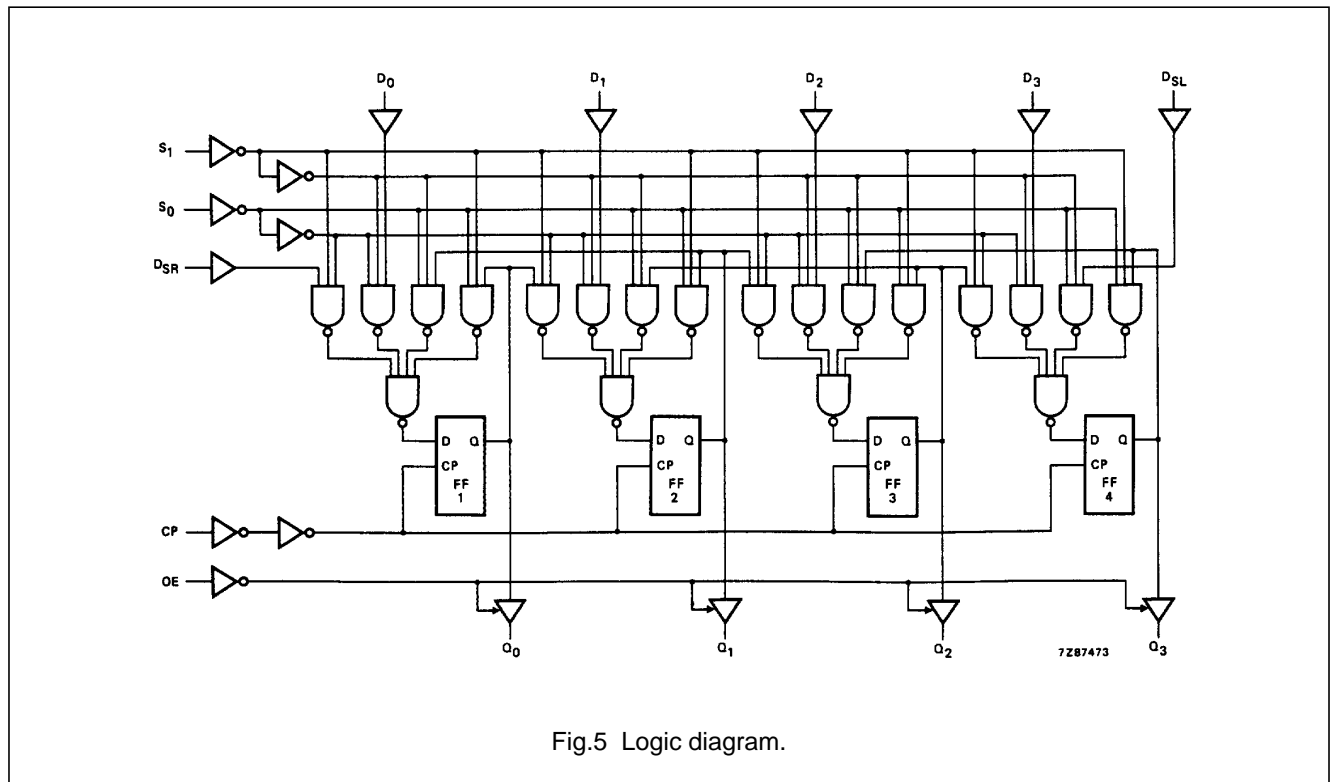


FUNCTION TABLE

OPERATING MODES	INPUTS (OE = HIGH)					OUTPUTS at $t_{n+1}$			
	S <sub>1</sub>	S <sub>0</sub>	D <sub>SR</sub>	D <sub>SL</sub>	D <sub>0</sub> to D <sub>3</sub>	Q <sub>0</sub>	Q <sub>1</sub>	Q <sub>2</sub>	Q <sub>3</sub>
reset	L	L	X	X	X	L	L	L	L
shift left	H	L	X	L	X	Q <sub>1</sub>	Q <sub>2</sub>	Q <sub>3</sub>	L
	H	L	X	H	X	Q <sub>1</sub>	Q <sub>2</sub>	Q <sub>3</sub>	H
shift right	L	H	L	X	X	L	Q <sub>0</sub>	Q <sub>1</sub>	Q <sub>2</sub>
	L	H	H	X	X	H	Q <sub>0</sub>	Q <sub>1</sub>	Q <sub>2</sub>
parallel load	H	H	X	X	L	L	L	L	L
	H	H	X	X	H	H	H	H	H

Notes

- H = HIGH voltage level  
L = LOW voltage level  
X = don't care  
 $t_{n+1}$  = state after next LOW-to-HIGH transition of CP



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## DC CHARACTERISTICS FOR 74HC

For the DC characteristics see *"74HC/HCT/HCU/HCMOS Logic Family Specifications"*.

Output capability: bus driver

I<sub>CC</sub> category: MSI

## AC CHARACTERISTICS FOR 74HC

GND = 0 V; t<sub>r</sub> = t<sub>f</sub> = 6 ns; C<sub>L</sub> = 50 pF

SYMBOL	PARAMETER	T <sub>amb</sub> (°C)						UNIT	TEST CONDITIONS		
		74HC							V <sub>CC</sub> (V)	WAVEFORMS	
		+25			-40 to +85		-40 to +125				
		min.	typ.	max.	min.	max.	min.				max.
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay CP to Q <sub>n</sub>		44 16 13	170 34 29		215 43 37		255 51 43	ns	2.0 4.5 6.0	Fig.6
t <sub>PZH</sub> / t <sub>PZL</sub>	3-state output enable time OE to Q <sub>n</sub>		33 12 10	150 30 26		190 38 33		225 45 38	ns	2.0 4.5 6.0	Fig.8
t <sub>PHZ</sub> / t <sub>PLZ</sub>	3-state output disable time OE to Q <sub>n</sub>		50 18 14	150 30 26		190 38 33		225 45 38	ns	2.0 4.5 6.0	Fig.8
t <sub>THL</sub> / t <sub>TLH</sub>	output transition time		14 5 4	60 12 10		75 15 13		90 18 15	ns	2.0 4.5 6.0	Fig.6
t <sub>W</sub>	clock pulse width HIGH or LOW	80 16 14	11 4 3		100 20 17		120 24 20		ns	2.0 4.5 6.0	Fig.6
t <sub>SU</sub>	set-up time D <sub>n</sub> , D <sub>SR</sub> , D <sub>SL</sub> to CP	80 16 14	17 6 5		100 20 17		120 24 20		ns	2.0 4.5 6.0	Fig.8
t <sub>SU</sub>	set-up time S <sub>0</sub> , S <sub>1</sub> to CP	80 16 14	22 8 6		100 20 17		120 24 20		ns	2.0 4.5 6.0	Fig.8
t <sub>H</sub>	hold time D <sub>n</sub> , D <sub>SR</sub> , D <sub>SL</sub> to CP	2 2 2	-8 -3 -2		2 2 2		2 2 2		ns	2.0 4.5 6.0	Fig.8
t <sub>H</sub>	hold time S <sub>0</sub> , S <sub>1</sub> to CP	2 2 2	-14 -5 -4		2 2 2		2 2 2		ns	2.0 4.5 6.0	Fig.8
f <sub>max</sub>	maximum clock pulse frequency	6.0 30 35	19 56 67		4.8 24 28		4.0 20 24		MHz	2.0 4.5 6.0	Fig.6

# 4-bit bidirectional universal shift register; 3-state

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## DC CHARACTERISTICS FOR 74HCT

For the DC characteristics see *"74HC/HCT/HCU/HCMOS Logic Family Specifications"*.

Output capability: bus driver

I<sub>CC</sub> category: MSI

### Note to HCT types

The value of additional quiescent supply current ( $\Delta I_{CC}$ ) for a unit load of 1 is given in the family specifications. To determine  $\Delta I_{CC}$  per input, multiply this value by the unit load coefficient shown in the table below.

INPUT	UNIT LOAD COEFFICIENT
D <sub>0</sub> to D <sub>3</sub>	0.35
D <sub>SR</sub> , D <sub>SL</sub>	0.35
CP	0.35
S <sub>0</sub> , S <sub>1</sub>	0.70
OE	1.40

## AC CHARACTERISTICS FOR 74HCT

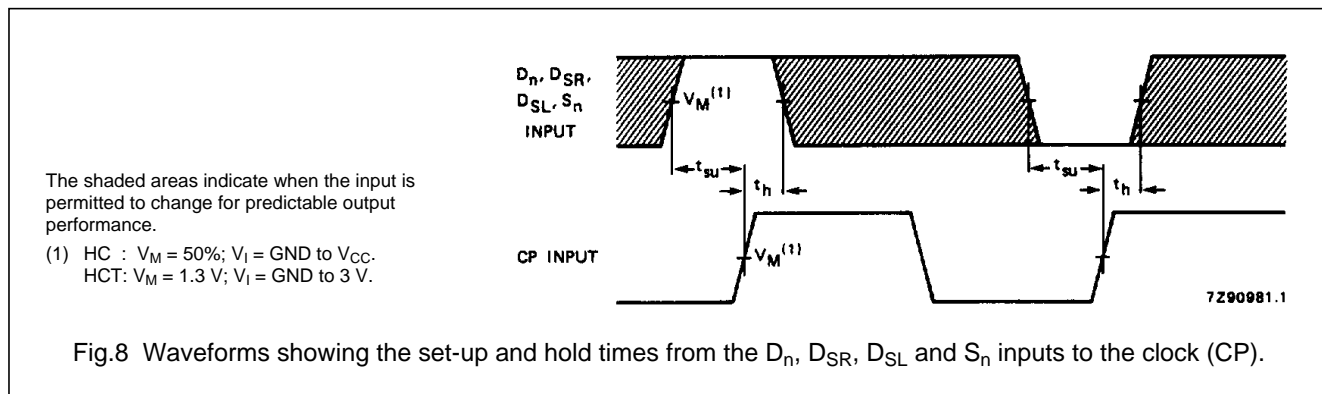
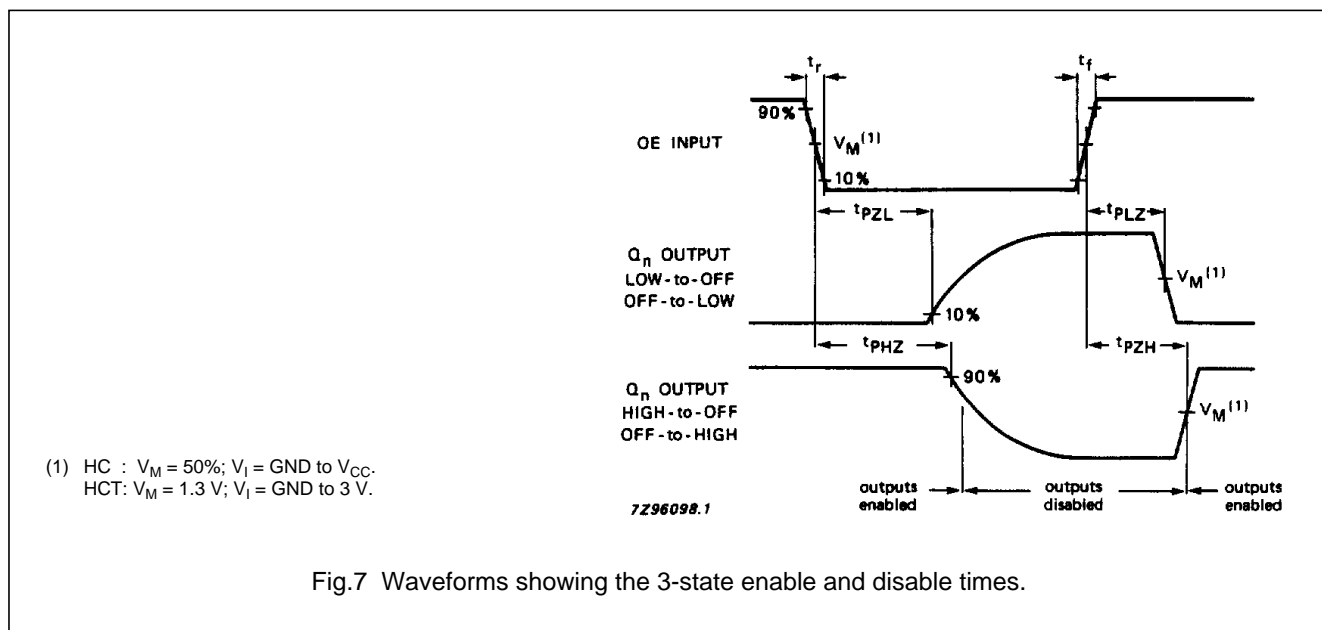
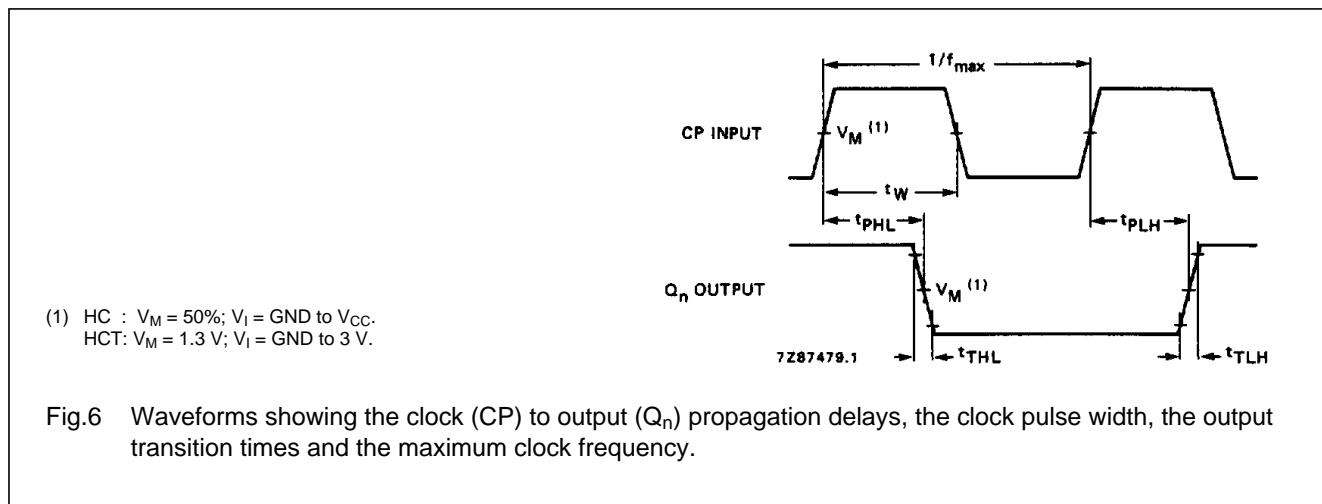
GND = 0 V; t<sub>r</sub> = t<sub>f</sub> = 6 ns; C<sub>L</sub> = 50 pF

SYMBOL	PARAMETER	T <sub>amb</sub> (°C)						UNIT	TEST CONDITIONS		
		74HCT							V <sub>CC</sub> (V)	WAVEFORMS	
		+25			-40 to +85		-40 to +125				
		min.	typ.	max.	min.	max.	min.				max.
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay CP to Q <sub>n</sub>		18	34		43		51	ns	4.5	Fig.6
t <sub>PZH</sub> / t <sub>PZL</sub>	3-state output enable time OE to Q <sub>n</sub>		12	30		38		45	ns	4.5	Fig.8
t <sub>PHZ</sub> / t <sub>PLZ</sub>	3-state output disable time OE to Q <sub>n</sub>		21	35		44		53	ns	4.5	Fig.8
t <sub>THL</sub> / t <sub>TLH</sub>	output transition time		5	12		15		18	ns	4.5	Fig.6
t <sub>W</sub>	clock pulse width HIGH or LOW	16	7		20		24		ns	4.5	Fig.6
t <sub>SU</sub>	set-up time D <sub>n</sub> , D <sub>SR</sub> , D <sub>SL</sub> to CP	16	8		20		24		ns	4.5	Fig.8
t <sub>SU</sub>	set-up time S <sub>0</sub> , S <sub>1</sub> to CP	20	9		25		30		ns	4.5	Fig.8
t <sub>H</sub>	hold time D <sub>n</sub> , D <sub>SR</sub> , D <sub>SL</sub> to CP	2	-2		2		2		ns	4.5	Fig.8
t <sub>H</sub>	hold time S <sub>0</sub> , S <sub>1</sub> to CP	2	-5		2		2		ns	4.5	Fig.8
f <sub>max</sub>	maximum clock pulse frequency	27	52		22		18		MHz	4.5	Fig.6

4-bit bidirectional universal shift register;  
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AC WAVEFORMS



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**PACKAGE OUTLINES**

See *"74HC/HCT/HCU/HCMOS Logic Package Outlines"*.