

## MM74C901 • MM74C902

### Hex Inverting TTL Buffer • Hex Non-Inverting TTL Buffer

#### General Description

The MM74C901 and MM74C902 hex buffers employ complementary MOS to achieve wide supply operating range, low power consumption, and high noise immunity. These buffers provide direct interface from PMOS into CMOS or TTL and direct interface from CMOS to TTL or CMOS operating at a reduced  $V_{CC}$  supply.

#### Features

- Wide supply voltage range: 3.0V to 15V
- Guaranteed noise margin: 1.0V
- High noise immunity:  $0.45 V_{CC}$  (typ.)
- TTL compatibility: Fan out of 2 driving standard TTL

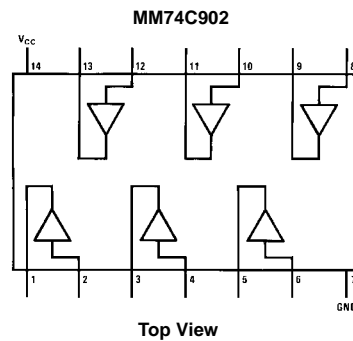
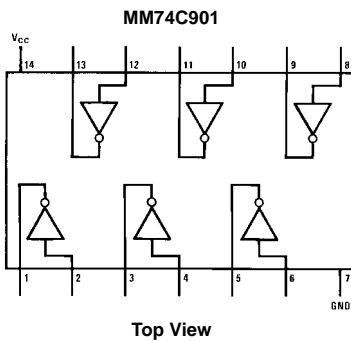
#### Ordering Code:

Order Number	Package Number	Package Description
MM74C901M	M14A	14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-120, 0.150" Narrow
MM74C901N	N14A	14-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-011, 0.300" Wide
MM74C902M	M14A	14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-120, 0.150" Narrow
MM74C902N	N14A	14-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-011, 0.300" Wide

Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

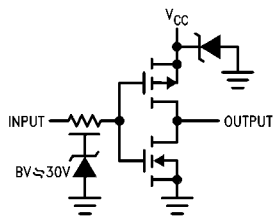
#### Connection Diagrams

Pin Assignments for DIP and SOIC

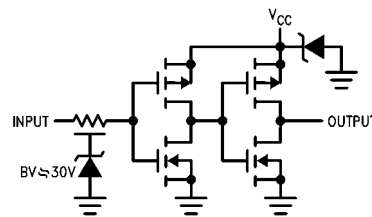


#### Logic Diagrams

**MM74C901**  
CMOS to TTL Inverting Buffer



**MM74C902**  
CMOS to TTL Buffer



<b>Absolute Maximum Ratings</b> (Note 1)		Operating $V_{CC}$ Range	3.0V to 15V
Voltage at Any Pin	-0.3V to $V_{CC} + 0.3V$	Absolute Maximum $V_{CC}$	18V
Voltage at Any Input Pin		Lead Temperature ( $T_L$ )	
MM74C901	-0.3V to +15V	(Soldering, 10 seconds)	260°C
MM74C902	-0.3V to +15V		
Storage Temperature Range ( $T_S$ )	-65°C to +150°C		
Power Dissipation ( $P_D$ )			
Dual-In-Line	700 mW		
Small Outline	500 mW		
Operating Temperature Range ( $T_A$ )			
MM74C901, MM74C902,	-40°C to +85°C		

**Note 1:** "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

## DC Electrical Characteristics

Min/Max limits apply across temperature range unless otherwise noted

Symbol	Parameter	Conditions	Min	Typ	Max	Units
<b>CMOS TO CMOS</b>						
$V_{IN(1)}$	Logical "1" Input Voltage	$V_{CC} = 5.0V$ $V_{CC} = 10V$	3.5 8.0			V V
$V_{IN(0)}$	Logical "0" Input Voltage	$V_{CC} = 5.0V$ $V_{CC} = 10V$			1.5 2.0	V V
$V_{OUT(1)}$	Logical "1" Output Voltage	$V_{CC} = 5.0V, I_O = -10 \mu A$ $V_{CC} = 10V, I_O = -10 \mu A$	4.5 9.0			V V
$V_{OUT(0)}$	Logical "0" Output Voltage	$V_{CC} = 5.0V$ $V_{CC} = 10V$			0.5 1.0	V V
$I_{IN(1)}$	Logical "1" Input Current	$V_{CC} = 15V, V_{IN} = 15V$		0.005	1.0	$\mu A$
$I_{IN(0)}$	Logical "0" Input Current	$V_{CC} = 15V, V_{IN} = 0V$	-1.0	-0.005		$\mu A$
$I_{CC}$	Supply Current	$V_{CC} = 15V$		0.05	15	$\mu A$
<b>TTL TO CMOS</b>						
$V_{IN(1)}$	Logical "1" Input Voltage	$V_{CC} = 4.75V$		$V_{CC} - 1.5$		V
$V_{IN(0)}$	Logical "0" Input Voltage	$V_{CC} = 4.75V$			0.8	V
<b>CMOS TO TTL</b>						
$V_{IN(1)}$	Logical "1" Input Voltage					
	MM74C901	$V_{CC} = 4.75V$	4.25			V
	MM74C902	$V_{CC} = 4.75V$	$V_{CC} - 1.5$			V
$V_{IN(0)}$	Logical "0" Input Voltage					
	MM74C901	$V_{CC} = 4.75V$			1.0	V
	MM74C902	$V_{CC} = 4.75V$			1.5	V
$V_{OUT(1)}$	Logical "1" Output Voltage	$V_{CC} = 4.75V, I_O = -800 \mu A$	2.4			V
$V_{OUT(0)}$	Logical "0" Output Voltage					
	MM74C901	$V_{CC} = 4.75V, I_O = 2.6 mA$			0.4	V
	MM74C902	$V_{CC} = 4.75V, I_O = 3.2 mA$			0.4	V
<b>OUTPUT DRIVE (See Family Characteristics Data Sheet) (Short Circuit Current)</b>						
<b>(MM74C901)</b>						
$I_{SOURCE}$	Output Source Current (P-Channel)	$V_{CC} = 5.0V, V_{OUT} = 0V$ $T_A = 25^\circ C, V_{IN} = 0V$	-5.0			mA
$I_{SOURCE}$	Output Source Current (P-Channel)	$V_{CC} = 10V, V_{OUT} = 0V$ $T_A = 25^\circ C, V_{IN} = 0V$	-20			mA
$I_{SINK}$	Output Sink Current (N-Channel)	$V_{CC} = 5.0V, V_{OUT} = V_{CC}$ $T_A = 25^\circ C, V_{IN} = V_{CC}$	9.0			mA
$I_{SINK}$	Output Sink Current (N-Channel)	$V_{CC} = 5.0V, V_{OUT} = 0.4V$ $T_A = 25^\circ C, V_{IN} = V_{CC}$	3.8			mA
<b>(MM74C902)</b>						

**DC Electrical Characteristics** (Continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
$I_{SOURCE}$	Output Source Current (P-Channel)	$V_{CC} = 5.0V, V_{OUT} = 0V$ $T_A = 25^\circ C, V_{IN} = V_{CC}$	-5.0			mA
$I_{SOURCE}$	Output Source Current (P-Channel)	$V_{CC} = 10V, V_{OUT} = 0V$ $T_A = 25^\circ C, V_{IN} = V_{CC}$	-20			mA
$I_{SINK}$	Output Sink Current (N-Channel)	$V_{CC} = 5.0V, V_{OUT} = V_{CC}$ $T_A = 25^\circ C, V_{IN} = 0V$	9.0			mA
$I_{SINK}$	Output Sink Current (N-Channel)	$V_{CC} = 5.0V, V_{OUT} = 0.4V$ $T_A = 25^\circ C, V_{IN} = 0V$	3.8			mA

**AC Electrical Characteristics** (Note 2)

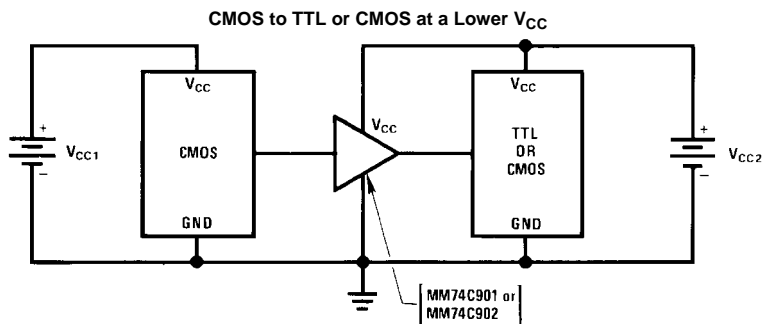
$T_A = 25^\circ C, C_L = 50$  pF, unless otherwise noted

Symbol	Parameter	Conditions	Min	Typ	Max	Units
<b>MM74C901</b>						
$t_{pd1}$	Propagation Delay Time to a Logical "1"	$V_{CC} = 5.0V$ $V_{CC} = 10V$		38 22	70 30	ns
$t_{pd0}$	Propagation Delay Time to a Logical "0"	$V_{CC} = 5.0V$ $V_{CC} = 10V$		21 13	35 20	ns
$C_{IN}$	Input Capacitance	Any Input (Note 3)		14		pF
$C_{PD}$	Power Dissipation Capacity	Per Buffer (Note 4)		30		pF
<b>MM74C902</b>						
$t_{pd1}$	Propagation Delay Time to a Logical "1"	$V_{CC} = 5.0V$ $V_{CC} = 10V$		57 27	90 40	ns
$t_{pd0}$	Propagation Delay Time to a Logical "0"	$V_{CC} = 5.0V$ $V_{CC} = 10V$		54 25	90 40	ns
$C_{IN}$	Input Capacitance	Any Input (Note 3)		5.0		pF
$C_{PD}$	Power Dissipation Capacity	Per Buffer (Note 4)		50		pF

**Note 2:** AC Parameters are guaranteed by DC correlated testing.

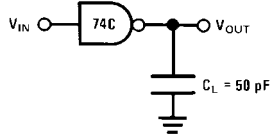
**Note 3:** Capacitance is guaranteed by periodic testing.

**Note 4:**  $C_{PD}$  determines the no load AC power consumption of any CMOS device. For complete explanation see Family Characteristics application note AN-90.

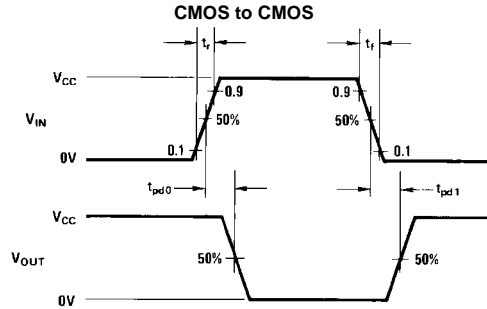
**Typical Application**

**Note:**  $V_{CC1} = V_{CC2}$

### AC Test Circuit and Switching Time Waveforms

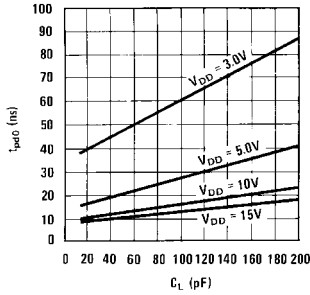


Note: Delays measured with input  $t_r, t_f = 20 \text{ ns}$ .

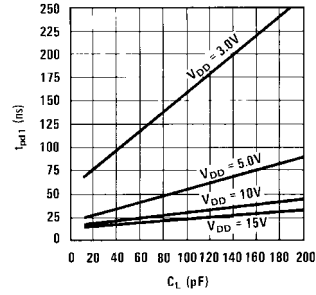


### Typical Performance Characteristics

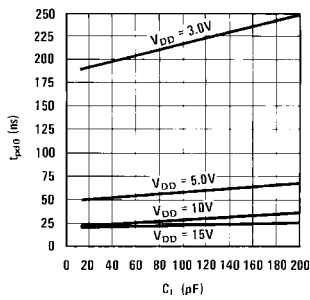
Typical Propagation Delay to a Logical "0" for the MM74C901



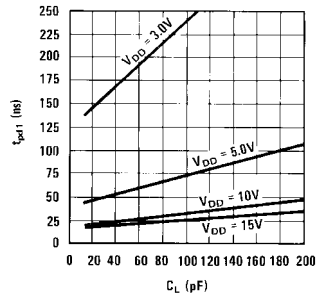
Typical Propagation Delay to a Logical "1" for the MM74C901



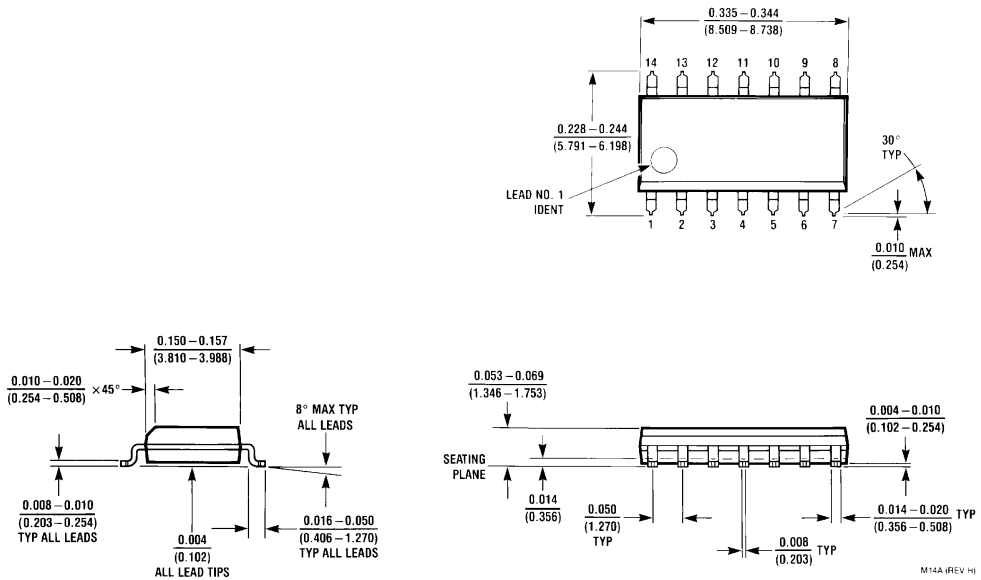
Typical Propagation Delay to a Logical "0" for the MM74C902



Typical Propagation Delay to a Logical "1" for the MM74C902



**Physical Dimensions** inches (millimeters) unless otherwise noted



**14-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-120, 0.150" Narrow  
Package Number M14A**

**Physical Dimensions** inches (millimeters) unless otherwise noted (Continued)



**14-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide Package Number N14A**

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