

MM74C85 4-Bit Magnitude Comparator

General Description

The MM74C85 is a four-bit magnitude comparator which will perform comparison of straight binary or BCD codes. The circuit consists of eight comparing inputs (A0, A1, A2, A3, B0, B1, B2, B3), three cascading inputs (A > B, A < B and A = B), and three outputs (A > B, A < B and A = B). This device compares two four-bit words (A and B) and determines whether they are "greater than," "less than," or "equal to" each other by a high level on the appropriate output. For words greater than four-bits, units can be cascaded by connecting the outputs (A > B, A < B, and A = B) of the least significant stage to the cascade inputs (A > B, A < B and A = B) of the next-significant stage. In addition the least significant stage must have a high level voltage

($V_{IN(1)}$) applied to the A = B input and low level voltage ($V_{IN(0)}$) applied to A > B and A < B inputs.

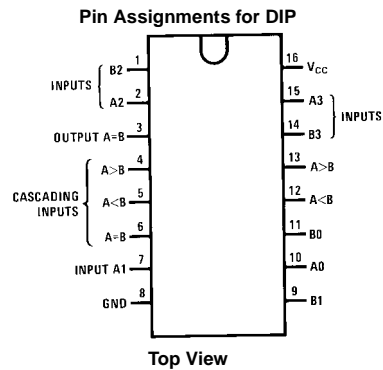
Features

- Wide supply voltage range: 3.0V to 15V
- Guaranteed noise margin: 1.0V
- High noise immunity: $0.4 V_{CC}$ (typ.)
- Low power: TTL compatibility:
fan out of 2 driving 74L
- Expandable to 'N' stages
- Applicable to binary or BCD
- Low power pinout: 74L85

Ordering Code:

Order Number	Package Number	Package Description
MM74C85N	N16E	16-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide

Connection Diagram

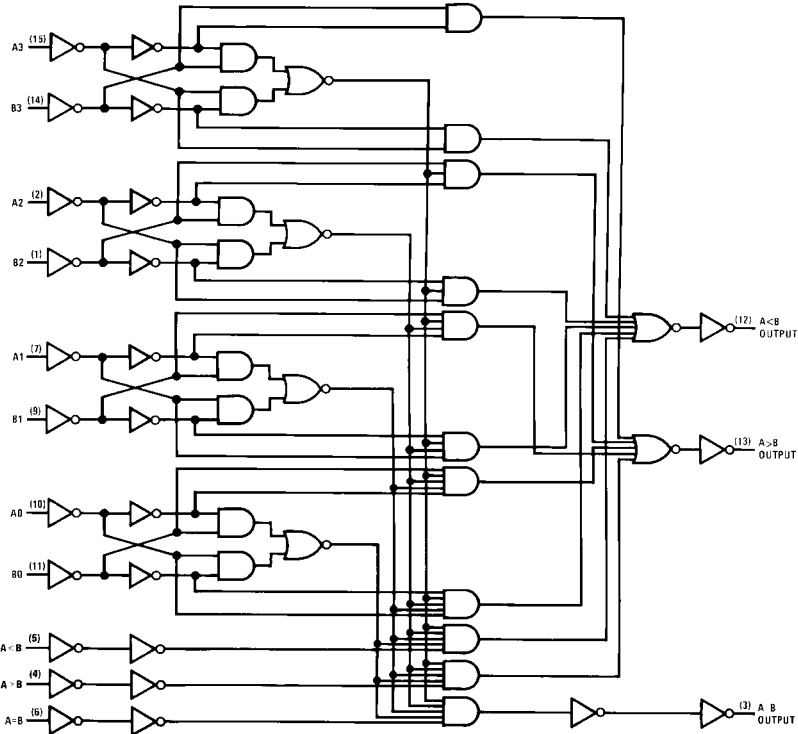


Truth Table

Comparing Inputs				Cascading Inputs			Outputs		
A3, B3	A2, B2	A1, B1	A0, B0	A > B	A < B	A = B	A > B	A < B	A = B
A3 > B3	X	X	X	X	X	X	H	L	L
A3 < B3	X	X	X	X	X	X	L	H	L
A3 = B3	A2 > B2	X	X	X	X	X	H	L	L
A3 = B3	A2 < B2	X	X	X	X	X	L	H	L
A3 = B3	A2 = B2	A1 > B1	X	X	X	X	H	L	L
A3 = B3	A2 = B2	A1 < B1	X	X	X	X	L	H	L
A3 = B3	A2 = B2	A1 = B1	A0 > B0	X	X	X	H	L	L
A3 = B3	A2 = B2	A1 = B1	A0 < B0	X	X	X	L	H	L
A3 = B3	A2 = B2	A1 = B1	A0 = B0	H	L	L	H	L	L
A3 = B3	A2 = B2	A1 = B1	A0 = B0	L	H	L	L	H	L
A3 = B3	A2 = B2	A1 = B1	A0 = B0	L	L	H	L	L	H
A3 = B3	A2 = B2	A1 = B1	A0 = B0	L	H	H	L	H	H
A3 = B3	A2 = B2	A1 = B1	A0 = B0	H	L	H	H	L	H
A3 = B3	A2 = B2	A1 = B1	A0 = B0	H	H	H	H	H	H
A3 = B3	A2 = B2	A1 = B1	A0 = B0	H	H	L	H	H	L
A3 = B3	A2 = B2	A1 = B1	A0 = B0	L	L	L	L	L	L

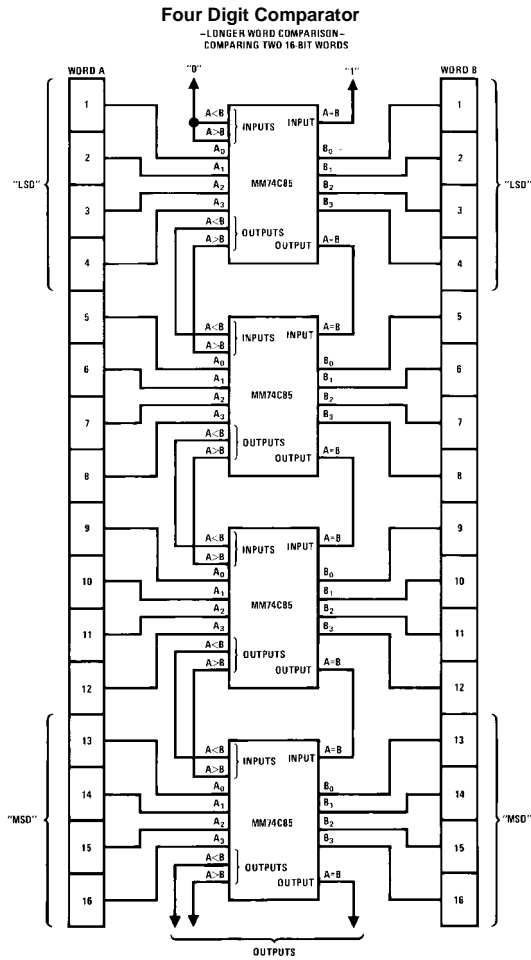
H = HIGH Level, L = LOW Level, X = Irrelevant

Logic Diagram

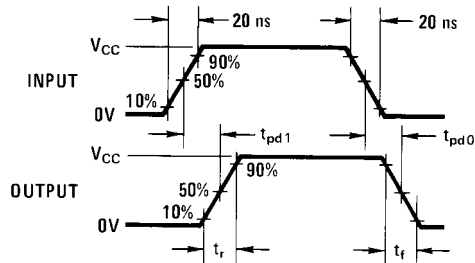


Absolute Maximum Ratings (Note 1)		V_{CC}	18V
Voltage at Any Pin	-0.3V to $V_{CC} + 0.3V$	Lead Temperature (Soldering, 10 seconds)	260°C
Operating Temperature Range	-40°C to +85°C		
Storage Temperature Range	-65°C to +150°C		
Power Dissipation (P_D)			
Dual-In-Line	700 mW		
Small Outline	500 mW		
Operating V_{CC} Range	3.0V to 15V		
Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.			
DC Electrical Characteristics			
Min/Max limits apply across temperature range unless otherwise noted			
Symbol	Parameter	Conditions	Units
CMOS TO CMOS			
$V_{IN(1)}$	Logical "1" Input Voltage	$V_{CC} = 5.0V$ $V_{CC} = 10V$	3.5 8.0 V V
$V_{IN(0)}$	Logical "0" Input Voltage	$V_{CC} = 5.0V$ $V_{CC} = 10V$	1.5 2.0 V V
$V_{OUT(1)}$	Logical "1" Output Voltage	$V_{CC} = 5.0V, I_O = -10 \mu A$ $V_{CC} = 10V, I_O = -10 \mu A$	4.5 9.0 V V
$V_{OUT(0)}$	Logical "0" Output Voltage	$V_{CC} = 5.0V, I_O = +10 \mu A$ $V_{CC} = 10V, I_O = +10 \mu A$	0.5 1.0 V V
$I_{IN(1)}$	Logical "1" Input Current	$V_{CC} = 15V, V_{IN} = 15V$	0.005 1.0 μA
$I_{IN(0)}$	Logical "0" Input Current	$V_{CC} = 15V, V_{IN} = 0V$	-1.0 -0.005 μA
I_{CC}	Supply Current	$V_{CC} = 15V$	0.05 300 μA
CMOS/LPTTL INTERFACE			
$V_{IN(1)}$	Logical "1" Input Voltage	$V_{CC} = 4.75V$	$V_{CC} - 1.5$ V
$V_{IN(0)}$	Logical "0" Input Voltage	$V_{CC} = 4.75V$	0.8 V
$V_{OUT(1)}$	Logical "1" Output Voltage	$V_{CC} = 4.75V, I_O = -360 \mu A$	2.4 V
$V_{OUT(0)}$	Logical "0" Output Voltage	$V_{CC} = 4.75V, I_O = 360 \mu A$	0.4 V
OUTPUT DRIVE (See Family Characteristics Data Sheet) (Short Circuit Current)			
I_{SOURCE}	Output Source Current (P-Channel)	$V_{CC} = 5.0V, V_{OUT} = 0V$ $T_A = 25^\circ C$	-1.75 -3.3 mA
I_{SOURCE}	Output Source Current (P-Channel)	$V_{CC} = 10V, V_{OUT} = 0V$ $T_A = 25^\circ C$	-8.0 -15 mA
I_{SINK}	Output Sink Current (N-Channel)	$V_{CC} = 5.0V, V_{OUT} = V_{CC}$ $T_A = 25^\circ C$	1.75 3.6 mA
I_{SINK}	Output Sink Current (N-Channel)	$V_{CC} = 10V, V_{OUT} = V_{CC}$ $T_A = 25^\circ C$	8.0 16 mA
AC Electrical Characteristics (Note 2)			
$T_A = 25^\circ C, C_L = 50 \text{ pF}$, unless otherwise specified			
Symbol	Parameter	Conditions	Units
t_{pd}	Propagation Delay from any A or B Data Input to any Data Output	$V_{CC} = 50V$ $V_{CC} = 10V$	250 100 ns ns
t_{pd}	Propagation Delay Time from any Cascade Input to any Output	$V_{CC} = 50V$ $V_{CC} = 10V$	200 100 ns ns
C_{IN}	Input Capacitance	Any Input	5.0 pF
C_{PD}	Power Dissipation Capacitance	Per Package (Note 4)	45 pF
Note 2: AC Parameters are guaranteed by DC correlated testing.			
Note 3: Capacitance is guaranteed by periodic testing.			
Note 4: C_{PD} determines the no load AC power consumption of any CMOS device. For complete explanation see Family Characteristics application note, AN-90.			

Typical Applications

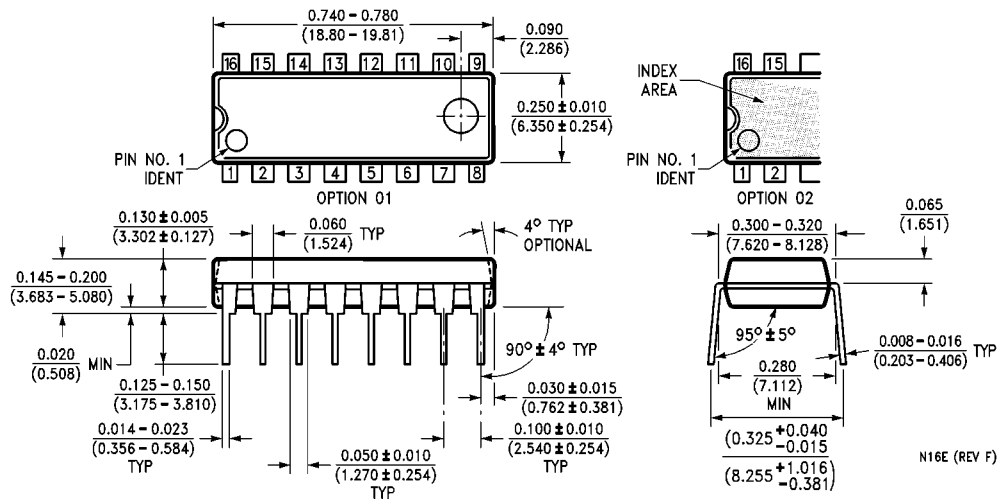


Switching Time Waveforms



Unused inputs must be tied to an appropriate logic level.

Physical Dimensions inches (millimeters) unless otherwise noted



16-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide Package Number N16E

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