

## MM54C195/MM74C195 4-Bit Registers

### General Description

The MM54C195/MM74C195 CMOS 4-bit registers feature parallel inputs, parallel outputs, J-K serial inputs, shift/load control input and a direct overriding clear. The following two modes of operation are possible:

#### Parallel Load

Shift in direction  $Q_A$  towards  $Q_D$

Parallel loading is accomplished by applying the four bits of data and taking the shift/load control of input low. The data is loaded into the associated flip-flops and appears at the outputs after the positive transition of the clock input. During parallel loading, serial data flow is inhibited.

Serial shifting is accomplished synchronously when the shift/load control input is high. Serial data for this mode is entered at the J-K inputs. These inputs allow the first stage to perform as a J-K, D, or T-type flip flop as shown in the truth table.

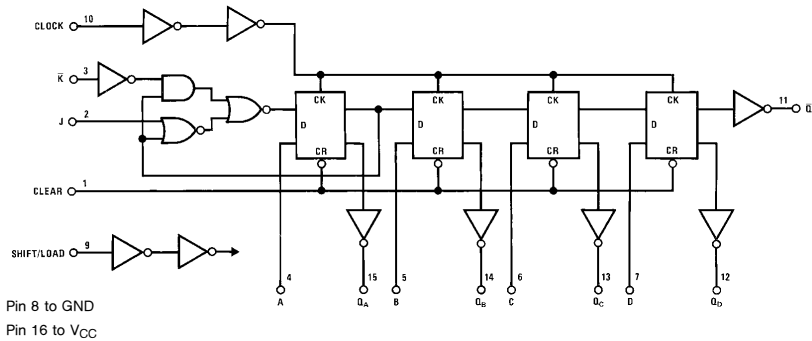
### Features

- Medium speed operation                      8.5 MHz (typ.) with 10V supply and 50 pF load
- High noise immunity                            0.45  $V_{CC}$  (typ.)
- Low power    100 nW (typ.)
- Tenth power TTL compatible                Drive 2 LPTTL loads
- Supply voltage range                            3V to 15V
- Synchronous parallel load
- Parallel inputs and outputs from each flip-flop
- Direct overriding clear
- J and K inputs to first stage
- Complementary outputs from last stage
- Positive-edge triggered clocking
- Diode clamped inputs to protect against static charge

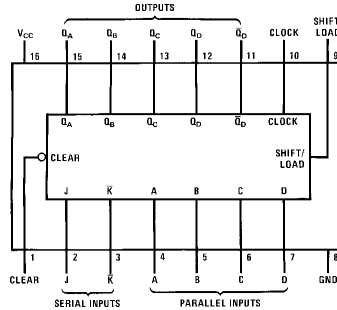
### Applications

- Automotive
- Data terminals
- Instrumentation
- Medical electronics
- Alarm systems
- Remote metering
- Industrial electronics
- Computers

### Schematic and Connection Diagrams



#### Dual-In-Line Package



## Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

|                             |                          |
|-----------------------------|--------------------------|
| Voltage at any Pin          | -0.3V to $V_{CC} + 0.3V$ |
| Operating Temperature Range | -55°C to +125°C          |
| MM54C195                    | -40°C to +85°C           |
| MM74C195                    |                          |

|                                       |                 |
|---------------------------------------|-----------------|
| Storage Temperature Range             | -65°C to +150°C |
| Power Dissipation ( $P_D$ )           |                 |
| Dual-In-Line                          | 700 mW          |
| Small Outline                         | 500 mW          |
| Operating $V_{CC}$ Range              | 3V to 15V       |
| Absolute Maximum $V_{CC}$             | 18V             |
| Lead Temperature (Soldering, 10 sec.) | 260°C           |

## DC Electrical Characteristics Min/Max limits apply across temperature range unless otherwise noted

| Symbol              | Parameter                  | Conditions                      | Min        | Typ    | Max        | Units   |
|---------------------|----------------------------|---------------------------------|------------|--------|------------|---------|
| <b>CMOS TO CMOS</b> |                            |                                 |            |        |            |         |
| $V_{IN(1)}$         | Logical "1" Input Voltage  | $V_{CC} = 5V$<br>$V_{CC} = 10V$ | 3.5<br>8.0 |        |            | V<br>V  |
| $V_{IN(0)}$         | Logical "0" Input Voltage  | $V_{CC} = 5V$<br>$V_{CC} = 10V$ |            |        | 1.5<br>2.0 | V<br>V  |
| $V_{OUT(1)}$        | Logical "1" Output Voltage | $V_{CC} = 5V$<br>$V_{CC} = 10V$ | 4.5<br>9.0 |        |            | V<br>V  |
| $V_{OUT(0)}$        | Logical "0" Output Voltage | $V_{CC} = 5V$<br>$V_{CC} = 10V$ |            |        | 0.5<br>1.0 | V<br>V  |
| $I_{IN(1)}$         | Logical "1" Input Current  | $V_{CC} = 15V$                  |            | 0.005  | 1.0        | $\mu A$ |
| $I_{IN(0)}$         | Logical "0" Input Current  | $V_{CC} = 15V$                  | -1.0       | -0.005 |            | $\mu A$ |
| $I_{CC}$            | Supply Current             | $V_{CC} = 15V$                  |            | 0.05   | 300        | $\mu A$ |

## CMOS/LPTTL INTERFACE

|              |                            |   |                                  |  |            |        |
|--------------|----------------------------|---|----------------------------------|--|------------|--------|
| $V_{IN(1)}$  | Logical "1" Input Voltage  | 54C $V_{CC} = 4.5V$<br>74C $V_{CC} = 4.75V$                                   | $V_{CC} - 1.5$<br>$V_{CC} - 1.5$ |  |            | V<br>V |
| $V_{IN(0)}$  | Logical "0" Input Voltage  | 54C $V_{CC} = 4.5V$<br>74C $V_{CC} = 4.75V$                                   |                                  |  | 0.8<br>0.8 | V<br>V |
| $V_{OUT(1)}$ | Logical "1" Output Voltage | 54C $V_{CC} = 4.5V, I_O = -360\mu A$<br>74C $V_{CC} = 4.75V, I_O = -360\mu A$ | 2.4<br>2.4                       |  |            | V<br>V |
| $V_{OUT(0)}$ | Logical "0" Output Voltage | 54C $V_{CC} = 4.5V, I_O = 360\mu A$<br>74C $V_{CC} = 4.75V, I_O = 360\mu A$   |                                  |  | 0.4<br>0.4 | V<br>V |

## OUTPUT DRIVE (See 54C/74C Family Characteristics Data Sheet) (Short Circuit Current)

|              |                       |   |       |  |  |    |
|--------------|-----------------------|---|-------|--|--|----|
| $I_{SOURCE}$ | Output Source Current | $V_{CC} = 5V, V_{IN(0)} = 0V$<br>$T_A = 25^\circ C, V_{OUT} = 0V$       | -1.75 |  |  | mA |
| $I_{SOURCE}$ | Output Source Current | $V_{CC} = 10V, V_{IN(0)} = 0V$<br>$T_A = 25^\circ C, V_{OUT} = 0V$      | -8.0  |  |  | mA |
| $I_{SINK}$   | Output Sink Current   | $V_{CC} = 5V, V_{IN(1)} = 5V$<br>$T_A = 25^\circ C, V_{OUT} = V_{CC}$   | 1.75  |  |  | mA |
| $I_{SINK}$   | Output Sink Current   | $V_{CC} = 10V, V_{IN(1)} = 10V$<br>$T_A = 25^\circ C, V_{OUT} = V_{CC}$ | 8.0   |  |  | mA |

**Note 1:** "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

## AC Electrical Characteristics\* $T_A = 25^\circ\text{C}$ , $C_L = 50\text{ pF}$ , unless otherwise noted

| Symbol     | Parameter   | Conditions            | Min | Typ  | Max | Units         |
|------------|---|-----------------------|-----|------|-----|---------------|
| $t_{pd}$   | Propagation Delay Time to a Logical "0" or Logical "1" from Clock to Q or $\bar{Q}$ | $V_{CC} = 5\text{V}$  |     | 150  | 300 | ns            |
|            |   | $V_{CC} = 10\text{V}$ |     | 75   | 130 | ns            |
| $t_{pd}$   | Propagation Delay Time to a Logical "0" or Logical "1" from Clear to Q or $\bar{Q}$ | $V_{CC} = 5\text{V}$  |     | 150  | 300 | ns            |
|            |   | $V_{CC} = 10\text{V}$ |     | 50   | 130 | ns            |
| $t_S$      | Time Prior to Clock Pulse that Data must be Present                                 | $V_{CC} = 5\text{V}$  |     | 80   | 200 | ns            |
|            |   | $V_{CC} = 10\text{V}$ |     | 35   | 70  | ns            |
| $t_S$      | Time Prior to Clock Pulse that Shift/Load must be Present                           | $V_{CC} = 5\text{V}$  |     | 110  | 150 | ns            |
|            |   | $V_{CC} = 10\text{V}$ |     | 60   | 90  | ns            |
| $t_H$      | Time After Clock Pulse that Data must be Held                                       | $V_{CC} = 5\text{V}$  |     | -10  | 0   | ns            |
|            |   | $V_{CC} = 10\text{V}$ |     | -5.0 | 0   | ns            |
| $t_W$      | Minimum Clear Pulse Width ( $t_{WL} = t_{WH}$ )                                     | $V_{CC} = 5\text{V}$  |     | 100  | 200 | ns            |
|            |   | $V_{CC} = 10\text{V}$ |     | 50   | 100 | ns            |
| $t_W$      | Minimum Clear Pulse Width   | $V_{CC} = 5\text{V}$  |     | 90   | 130 | ns            |
|            |   | $V_{CC} = 10\text{V}$ |     | 40   | 60  | ns            |
| $t_r, t_f$ | Maximum Clock Rise and Fall Time  | $V_{CC} = 5\text{V}$  | 5.0 |      |     | $\mu\text{s}$ |
|            |   | $V_{CC} = 10\text{V}$ | 2.0 |      |     | $\mu\text{s}$ |
| $f_{MAX}$  | Maximum Input Clock Frequency   | $V_{CC} = 5\text{V}$  | 2.0 | 3.0  |     | MHz           |
|            |   | $V_{CC} = 10\text{V}$ | 5.5 | 8.5  |     | MHz           |
| $C_{IN}$   | Input Capacitance   | (Note 2)              |     | 5.0  |     | pF            |
| $C_{PD}$   | Power Dissipation Capacitance   | (Note 3)              |     | 100  |     | pF            |

\*AC Parameters are guaranteed by DC correlated testing.

**Note 1:** "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

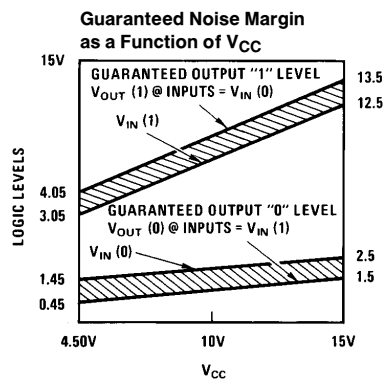
**Note 2:** Capacitance is guaranteed by periodic testing.

**Note 3:**  $C_{PD}$  determines the no load AC power consumption of any CMOS device. For complete explanation see 54C/74C Family Characteristics application note AN-90.

## Truth Table

| Inputs AT $t_n$ |           | Outputs AT $t_{n+1}$ |          |          |          |                |
|-----------------|-----------|----------------------|----------|----------|----------|----------------|
| J               | $\bar{K}$ | $Q_A$                | $Q_B$    | $Q_C$    | $Q_D$    | $\bar{Q}_D$    |
| L               | H         | $Q_{An}$             | $Q_{An}$ | $Q_{Bn}$ | $Q_{Cn}$ | $\bar{Q}_{Cn}$ |
| L               | L         | L                    | $Q_{An}$ | $Q_{Bn}$ | $Q_{Cn}$ | $\bar{Q}_{Cn}$ |
| H               | H         | H                    | $Q_{An}$ | $Q_{Bn}$ | $Q_{Cn}$ | $\bar{Q}_{Cn}$ |
| H               | L         | $\bar{Q}_{An}$       | $Q_{An}$ | $Q_{Bn}$ | $Q_{Cn}$ | $\bar{Q}_{Cn}$ |

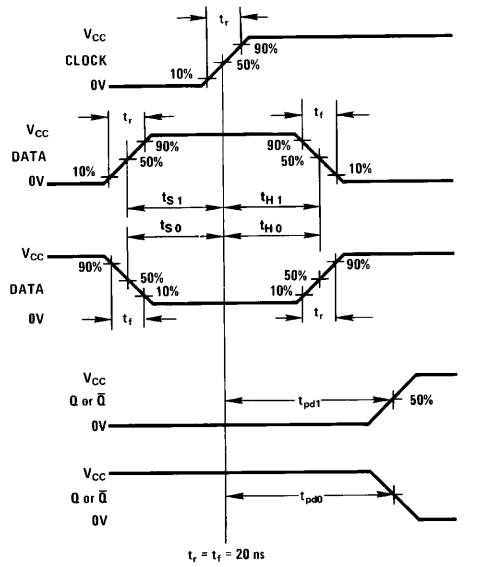
**Note:** H = High Level, L = Low Level  
 $t_n$  = bit time before clock pulse  
 $t_{n+1}$  = bit time after clock pulse  
 $Q_{An}$  = State of  $Q_A$  at  $t_n$



TL/F/5902-3

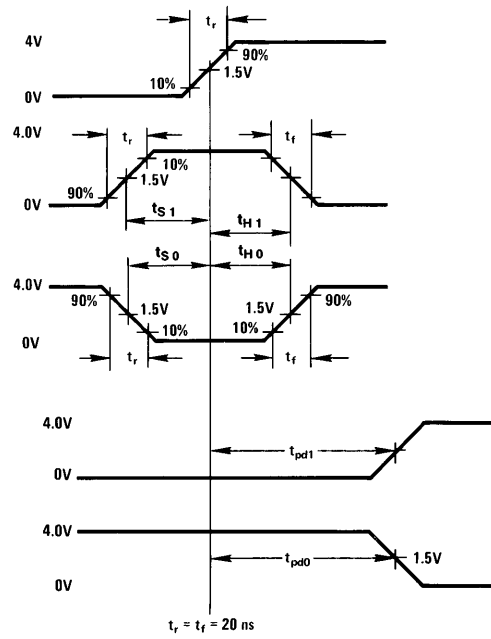
# Switching Time Waveforms

## CMOS to CMOS



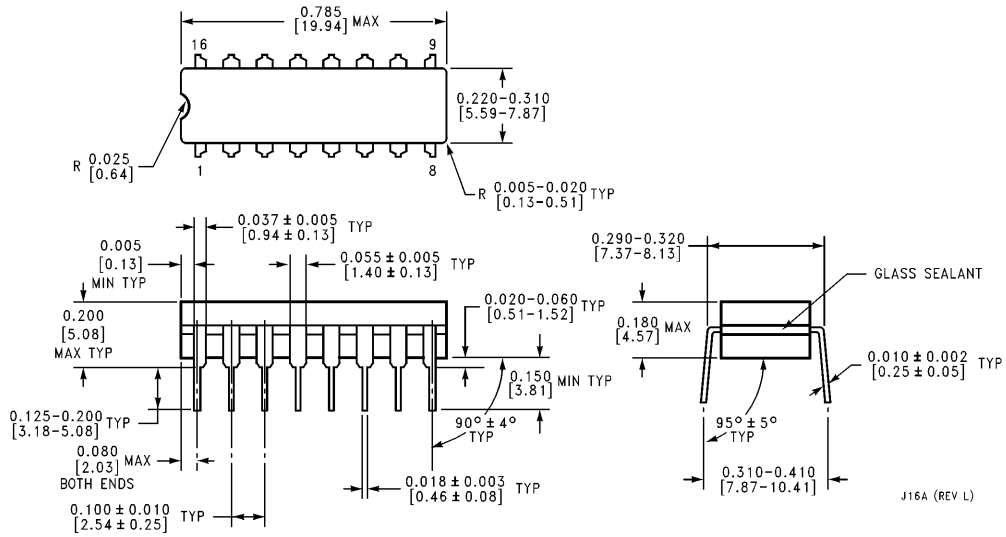
TL/F/5902-4

## TTL to CMOS



TL/F/5902-5

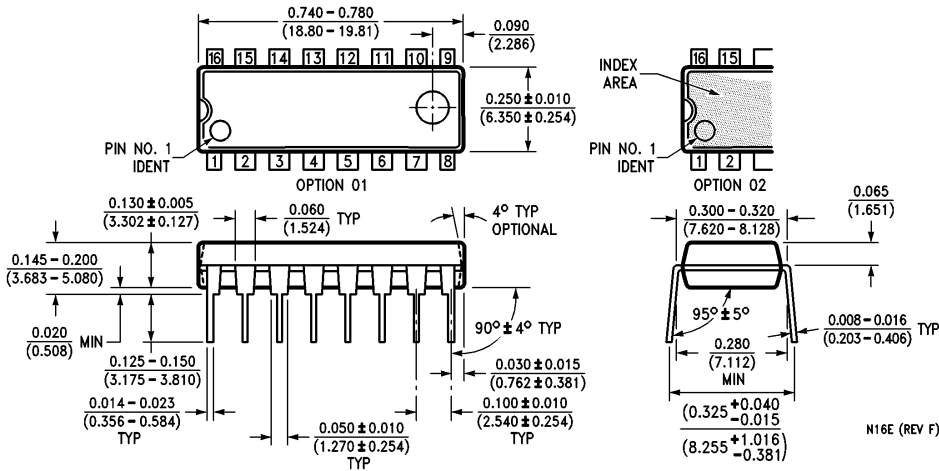
**Physical Dimensions** inches (millimeters)



**Ceramic Dual-In-Line Package (J)**  
**Order Number MM54C195J or MM74C195J**  
**NS Package Number J16A**

J16A (REV L)

**Physical Dimensions** inches (millimeters) (Continued)



**Molded Dual-In-Line Package (N)**  
**Order Number MM54C195N or MM74C195N**  
**NS Package Number N16E**

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