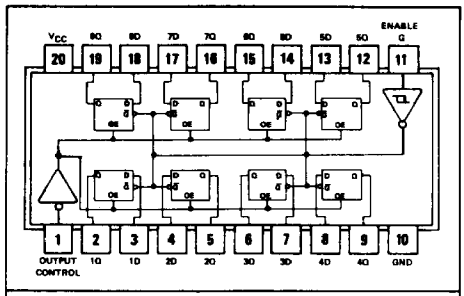
TYPES SN54LS363, SN54LS364, SN74LS363, SN74LS364
OCTAL D-TYPE TRANSPARENT LATCHES AND EDGE-TRIGGERED FLIP-FLOPS

BULLETIN NO. DL-S 7612466, OCTOBER 1976

- High V_{OH} . . . 3.65 V Min (74LS')
- Choice of 8 Latches or 8 D-Type Flip-Flops In a Single Package
- 3-State Bus-Driving Outputs
- Full Parallel-Access for Loading and Reloading
- Buffered Control Inputs
- Clock/Enable Input Has Hysteresis to Improve Noise Rejection and P-N-P Inputs To Reduce D-C Loading
- SN54LS373/SN74LS373 and SN54LS374/ SN74LS374 Are Similar But Have Standard V_{OH} of 2.4 V Min

SN54LS363 . . . J PACKAGE
SN74LS363 . . . J OR N PACKAGE
(TOP VIEW)

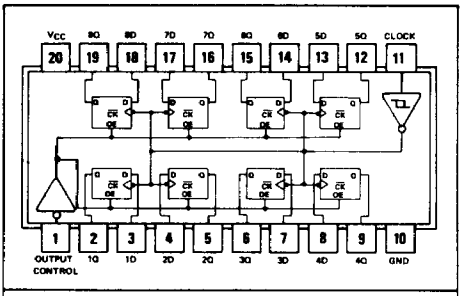


logic: see function table

'LS363
FUNCTION TABLE

OUTPUT CONTROL	ENABLE G	D	OUTPUT
L	H	H	H
L	H	L	L
L	L	X	Q_0
H	X	X	Z

SN54LS364 . . . J PACKAGE
SN74LS364 . . . J OR N PACKAGE
(TOP VIEW)



logic: see function table

'LS364
FUNCTION TABLE

OUTPUT CONTROL	CLOCK	D	OUTPUT
L	↑	H	H
L	↑	L	L
L	L	X	Q_0
H	X	X	Z

See explanation of function tables on page 3-8.

description

These 8-bit registers feature totem-pole three-state outputs designed specifically for driving highly-capacitive or relatively low-impedance loads. The high-impedance third state and increased high-logic-level drive provide these registers with the capability of being connected directly to and driving the bus lines in a bus-organized system without need for interface or pull-up components. They are particularly attractive for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

The eight latches of the 'LS363 are transparent D-type latches meaning that while the enable (G) is high the Q outputs will follow the data (D) inputs. When the enable is taken low the outputs will be latched at the level of the data that was setup.

The eight flip-flops of the 'LS364 are edge-triggered D-type flip-flops. On the positive transition of the clock the Q output will be set to the logic state that was setup at the D input. The 'LS363 is particularly useful for interfacing to MOS logic where a higher than normal V_{OH} level is desirable such as that required by the TMS 8080A microprocessor.

Schmitt-trigger buffered inputs at the enable ('LS363) and clock ('LS364) lines simplify system design as ac and dc noise rejection is improved by typically 400 mV due to the input hysteresis. A buffered output control input can be used to place the eight outputs in either a normal logic state (high or low logic levels) or a high-impedance state. In the high-impedance state the outputs neither load nor drive the bus line significantly.

DESIGN GOAL

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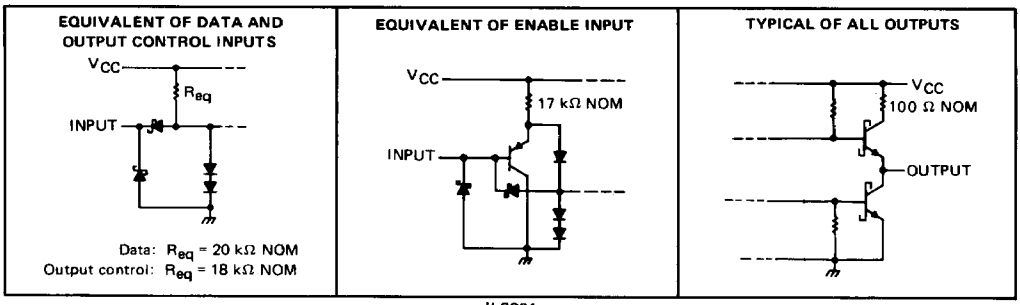
TYPES SN54LS363, SN54LS364, SN74LS363, SN74LS364
OCTAL D-TYPE TRANSPARENT LATCHES AND EDGE-TRIGGERED FLIP-FLOPS

functional block diagram

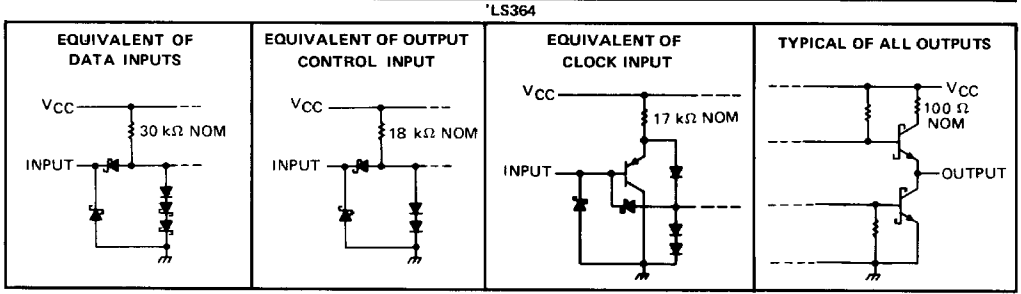
Same as SN54LS373/SN74LS373 and SN54LS374/SN74LS374

schematics of inputs and outputs

'LS363



'LS364



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

7

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage . . . . . 7 V
Off-state output voltage . . . . . 7 V
Operating free-air temperature range: SN54LS' . . . . . −55°C to 125°C
SN74LS' . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

recommended operating conditions

		SN54LS'			SN74LS'			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}		4.5	5	5.5	4.75	5	5.25	V
High-level output voltage, V_{OH}				5.5			5.5	V
High-level output current, I_{OH}				−1			−2.6	mA
Width of clock/enable pulse, t_w	High	15			15			ns
	Low	15			15			
Data setup time, t_{su}	'LS363	0↓			0↓			ns
	'LS364	20↑			20↑			
Data hold time, t_h	'LS363	10↓			10↓			ns
	'LS364	0↑			0↑			
Operating free-air temperature, T_A		−55		125	0		70	°C

↑↓ The arrow indicates the transition of the clock/enable input used for reference: ↑ for the low-to-high transition, ↓ for the high-to-low transition.

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		SN54LS'			SN74LS'			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH}	High-level input voltage			2			2			V
V_{IL}	Low-level input voltage					0.7			0.8	V
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = −18 mA				−1.5			−1.5	V
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = V_{IL}max, I_{OH} = MAX		3.45			3.65			V
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = V_{IL}max	I_{OL} = 12 mA		0.25	0.4		0.25	0.4	V
			I_{OL} = 24 mA					0.35	0.5	
I_{OZH}	Off-state output current, high-level voltage applied	V_{CC} = MAX, V_{IH} = 2 V, V_O = 3.65 V				20			20	μA
I_{OZL}	Off-state output current, low-level voltage applied	V_{CC} = MAX, V_{IH} = 2 V, V_O = 0.4 V				−20			−20	μA
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 7 V				0.1			0.1	mA
I_{IH}	High-level input current	V_{CC} = MAX, V_I = 2.7 V				20			20	μA
I_{IL}	Low-level input current	V_{CC} = MAX, V_I = 0.4 V				−400			−400	μA
I_{OS}	Short-circuit output current§	V_{CC} = MAX		−30		−130	−30		−130	mA
I_{CC}	Supply current	V_{CC} = MAX, Output control at 4.5 V			42	70		42	70	mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.
§ Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	'LS363			'LS364			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
f_{max}			C_L = 45 pF, R_L = 667 Ω, See Notes 2 and 3				35	50		MHz
t_{PLH}	Data	Any Q			15	23				ns
t_{PHL}					18	27				
t_{PLH}	Clock or enable	Any Q			19	30		21	33	ns
t_{PHL}					24	36		22	34	
t_{PZH}	Output Control	Any Q			16	28		16	28	ns
t_{PZL}					22	36		22	36	
t_{PHZ}	Output Control	Any Q	C_L = 5 pF, R_L = 667 Ω, See Note 3		12	20		10	18	ns
t_{PLZ}					16	25		14	24	

NOTES: 2. Maximum clock frequency is tested with all outputs loaded.
3. See load circuits and waveforms on page 3-11.

f_{max} ≡ maximum clock frequency
t_{PLH} ≡ propagation delay time, low-to-high-level output
t_{PHL} ≡ propagation delay time, high-to-low-level output
t_{PZH} ≡ output enable time to high level
t_{PZL} ≡ output enable time to low level
t_{PHZ} ≡ output disable time from high level
t_{PLZ} ≡ output disable time from low level

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DESIGN GOAL

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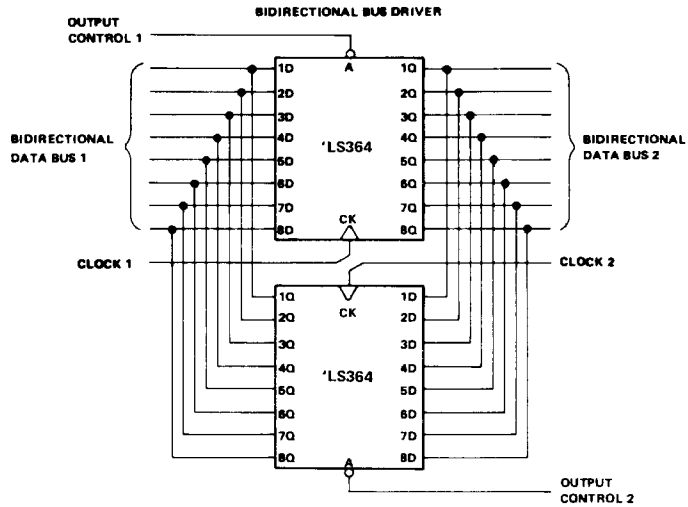
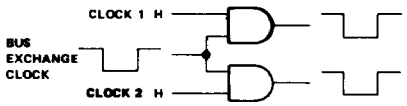
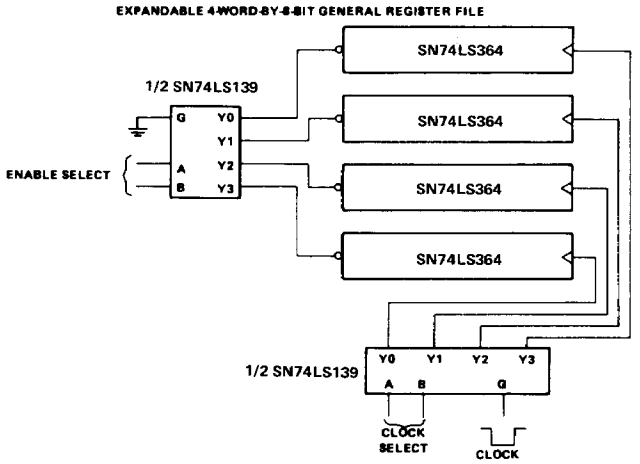
TYPICAL APPLICATION DATA





CLOCK CIRCUIT FOR BUS EXCHANGE



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