DATA SHEET

For a complete data sheet, please also download:

- The IC04 LOCMOS HE4000B Logic Family Specifications HEF, HEC
- The IC04 LOCMOS HE4000B Logic Package Outlines/Information HEF, HEC

HEF4531B
MSI
13-input parity checker/generator

Product specification
File under Integrated Circuits, IC04

January 1995

Philips Semiconductors

PHILIPS

13-input parity checker/generator

HEF4531B
MSI

DESCRIPTION

The HEF4531B is a parity checker/generator with 13 parity inputs (I_0 to I_{12}) and a parity output (O). When the number of parity inputs that are HIGH is even, the output is LOW. When the number of parity inputs that are HIGH is odd, the output is HIGH. For words of 12 bits or less, the output can be used to generate either odd or even parity by appropriate termination of the unused parity input(s). For words of 14 or more bits, the devices can be cascaded by connecting the output of one device to any parity input of another device. When cascading devices, it is recommended that the output of one device be connected to the I_{12} input of the other device since there is less delay to the output from the I_{12} input than from any other input (I_0 to I_{11}).

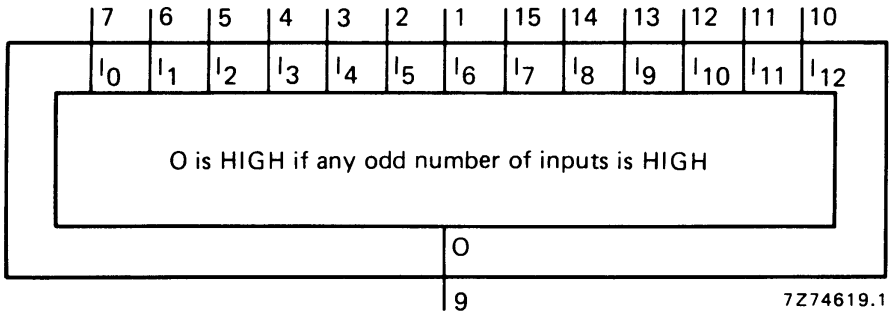

Fig.1 Functional diagram.

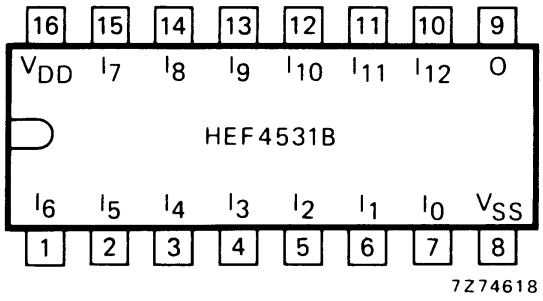

Fig.2 Pinning diagram.

HEF4531BP(N): 16-lead DIL; plastic (SOT38-1)

HEF4531BD(F): 16-lead DIL; ceramic (cerdip) (SOT74)

HEF4531BT(D): 16-lead SO; plastic (SOT109-1)

( ): Package Designator North America

FAMILY DATA, I_{DD} LIMITS category MSI

See Family Specifications

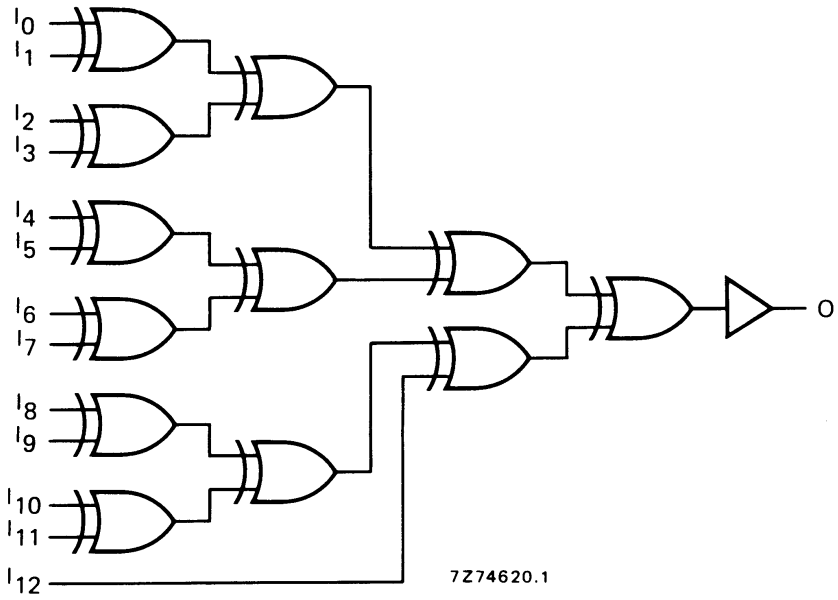

Fig.3 Logic diagram.

FUNCTION TABLE

INPUTS													OUTPUT
I_0	I_1	I_2	I_3	I_4	I_5	I_6	I_7	I_8	I_9	I_{10}	I_{11}	I_{12}	O
L	L	L	L	L	L	L	L	L	L	L	L	L	L
any odd number of inputs HIGH													H
any even number of inputs HIGH													L
H	H	H	H	H	H	H	H	H	H	H	H	H	H

Notes

1. H = HIGH state (the more positive voltage)
2. L = LOW state (the less positive voltage)

AC CHARACTERISTICS

V_{SS} = 0 V; T_{amb} = 25 °C; input transition times ≤ 20 ns

	V_{DD} V	TYPICAL FORMULA FOR P (μW)	
Dynamic power dissipation per package (P)	5	$425\ f_i + \sum (f_o C_L) \times V_{DD}^2$	where f_i = input freq. (MHz) f_o = output freq. (MHz) C_L = load capacitance (pF) $\sum (f_o C_L)$ = sum of outputs V_{DD} = supply voltage (V)
	10	$2\ 400\ f_i + \sum (f_o C_L) \times V_{DD}^2$	
	15	$7\ 700\ f_i + \sum (f_o C_L) \times V_{DD}^2$	

AC CHARACTERISTICS

V_{SS} = 0 V; T_{amb} = 25 °C; C_L = 50 pF; input transition times ≤ 20 ns

	V_{DD} V	SYMBOL	TYP.	MAX.		TYPICAL EXTRAPOLATION FORMULA
Propagation delays						
I_0 to $I_{11} \rightarrow O$	5		145	290	ns	118 ns + (0,55 ns/pF) C_L
HIGH to LOW	10	t_{PHL}	60	120	ns	49 ns + (0,23 ns/pF) C_L
	15		45	90	ns	37 ns + (0,16 ns/pF) C_L
	5		135	270	ns	108 ns + (0,55 ns/pF) C_L
LOW to HIGH	10	t_{PLH}	55	110	ns	44 ns + (0,23 ns/pF) C_L
	15		45	90	ns	37 ns + (0,16 ns/pF) C_L
$I_{12} \rightarrow 0$	5		105	210	ns	78 ns + (0,55 ns/pF) C_L
HIGH to LOW	10	t_{PHL}	45	90	ns	34 ns + (0,23 ns/pF) C_L
	15		35	70	ns	27 ns + (0,16 ns/pF) C_L
	5		85	170	ns	58 ns + (0,55 ns/pF) C_L
LOW to HIGH	10	t_{PLH}	35	70	ns	24 ns + (0,23 ns/pF) C_L
	15		25	50	ns	17 ns + (0,16 ns/pF) C_L
Output transition times	5		60	120	ns	10 ns + (1,0 ns/pF) C_L
HIGH to LOW	10	t_{THL}	30	60	ns	9 ns + (0,42 ns/pF) C_L
	15		20	40	ns	6 ns + (0,28 ns/pF) C_L
	5		60	120	ns	10 ns + (1,0 ns/pF) C_L
LOW to HIGH	10	t_{TLH}	30	60	ns	9 ns + (0,42 ns/pF) C_L
	15		20	40	ns	6 ns + (0,28 ns/pF) C_L